Design and Characterization of Selectively Functionalized Nanoscale Electronic Devices

by
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ABSTRACT
KWAN SKINNER: Design and Characterization of Selectively Functionalized Nanoscale Electronic Devices.
(Under the direction of Sean Washburn.)

This dissertation is a continuation of an earlier work on the theory and fabrication of a massively parallel self-assembled computer architecture. Specifically, this work focuses on some aspects of the fabrication of such architectures, with special focus on the design and fabrication of the active nanoscale components of this system. To this end, a nanoscale transistor has been fabricated and its electrical properties have been examined and improved upon. DNA-directed integration of these structures with nanoscale scaffolds in an addressable manner via self-assembly techniques is also addressed via a functionalization scheme that was devised to allow the arbitrary attachment of self-assembled monolayers anywhere along the length of these nanostructures.

This dissertation also illustrates how diverse a single designed nanoscale object can be and how the lines of chemistry, physics and materials science truly become blurred at a scales on the order of 10^{-9} m. Heterostructured nanowires that were originally only meant to act as active elements in nanoscale computer circuitry have been shown to behave as excellent nanoscale sensors for both self-assembled monolayers (SAMs) and gas analytes, and the same elements are now also known to act as coupling devices for free-space photons to the surface plasmon modes of the nanowire. These sensors and photonic wave guides also act as excellent recipients for selective functionalization schemes of arbitrary regions anywhere along its length, which opens up numerous av-

enues for different uses, potentially ranging from biological applications to multiplexing experiments.

Mechanical measurements on these heterostructured nanowires have also been performed and compared quantitatively to other structures that may be chosen as candidates for active or passive components a self-assembled system. These mechanical and electrical properties can be used to make educated decisions about how components integrated with the scaffolds to form larger computational elements will behave, and provides essential information needed for future experiments that will produce composite structures from these components.

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List of Abbreviations

- AAO - anodic aluminum oxide
- AFM - atomic force microscop(e/py)
- CNT - carbon nanotubes
- CV - cyclic voltammogram
- DNA - Deoxyribonucleic acid
- EIS - electrochemical impedance spectroscopy
- EUV - extreme ultraviolet
- FET - field-effect-transistor
- I-V - current-voltage
- MFM - magnetic force microscopy
- MPTMS - (3-mercaptopropyl)trimethoxysilane
- MSM - metal-semiconductor-metal
- NW - nanowire
- PA - porous aluminum

- PCTE - polycarbonate track etched
- PMMA - poly(methyl methacrylate)
- PVP - poly(vinylpyrrolidone)
- Q1D - quasi-one-dimensional
- SAM - self-assembled monolayer
- SEM - scanning electron microscop(e/py)
- SERS - surface enhanced raman spectroscopy
- SPM - scanning probe microscopy
- STM - scanning tunneling microscopy
- TE - thermionic emission
- TEM - transmission electron microscop(e/py)
- TFE - thermionic field emission
- USD - United States Dollars
- UV - ultraviolet

"Humanity has the stars in its future, and that future is too important to be lost under the burden of juvenile folly and ignorant superstition." – Isaac Asimov

Chapter 1

Introduction

1.1 Overview

Although nanotechnology is largely in its infancy when compared to other more established technologies, it is already finding practical use in applications ranging from those as specific as water filtration to consumer products. In recent years, the computing and electronics industries in particular have both expressed significant interest in integrating current developments in nanotechnology with manufacturing processes and facilities already in place as the desire to create faster computers with higher transistor density continues to grow. The rate of adoption of these new developments will be largely dependent on the demonstration of their potential usefulness in end-product applications, which will largely depend on characterization of materials properties such as electrical, chemical and mechanical characteristics. This dissertation presents efforts towards this goal through the design and characterization (electrically and mechanically) of heterostructured nanowires which are intended for integration with nanoscale DNA scaffolds in order to show that these structures are viable candidates for active

elements in future nanoscale electronics and computing applications.

1.2 Thesis statement and contributions

This thesis presents an argument on the usefulness of heterostructured nanowires as potential active elements in future computer circuitry. Specifically, the electrical and mechanical properties of these structures are evaluated, and a scheme to attach different types of molecules to different locations selectively along the length of the nanowire is presented. In the chapters that follow, results from experiments are presented that conveys the feasibility of these nanoscale elements to act as active and passive devices in future self-assembled architectures.

The electrical and mechanical properties obtained from heterostructured devices constructed here are important parameters needed when considering the functionality desired in architectures composed of large numbers these components. Additionally, the arbitrary attachment of various monolayers (specifically DNA) along the length of these structures will be critical for the directed self-assembly of these systems, as traditional write-based methods will no longer be feasible or practical. Based on the wide range of topics addressed in this dissertation, the information here contributes directly to the fields of materials science and physics, with minor contributions to chemistry as well.

1.3 Outline

This work is organized as follows: Chapter 2 presents a brief overview of current computer fabrication technologies and the capabilities of products produced by these technologies in terms of feature size. A brief synopsis of self-assembled DNA lattice technology is also included as it is anticipated to guide the assembly of smaller, future electronic devices, along with a high-level view of the different types of nanowires and other quasi-one-dimensional structures that have been fabricated thus far which may be potential candidates for attaching to these lattice structures. An overview of the types of electrical and mechanical experiments that have been conducted on these elements is also included for completeness.

Chapter 3 presents results obtained from the fabrication of electroless and electrochemically deposited single-material nanowires. An evaluation of which is more suitable for device integration with future architectures is also presented. In addition, findings on arbitrary nanowire functionalization is also presented here, as these functionalization schemes are expected to play a crucial role in subsequent assembly schemes. Chapter 4 discusses the electrical characteristics of these devices, and presents a generalized method that may be useful in the increase of majority carrier mobilities in these devices. Chapter 5 explores the mechanical stability and robustness of these nanostructures. Finally, chapter 6 summarizes these findings and discusses directions for future research in these areas.

Chapter 2

Related work

2.1 State of the art computer fabrication overview

Advances in processor fabrication over the last 40 years has followed a trend that has universally been labeled as Moore's Law. This law is frequently misquoted and misinterpreted as the doubling of a processor's speed and power every 18 to 24 months. In reality, this law is in fact about the density of the number of transistors per unit area which has no bearing on how those transistors are used in the final product.

The actual law was first summarized as follows by Gordon Moore in a 1965 issue of Electronics Magazine well before it was formulated as a law by Caltech professor Carver Mead and subsequently became a governing statement:

> "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year...Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe

> it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer."(Gardiner, 2007)

Thus under Moore's law, the number of transistors increase geometrically which typically (but not always) results in double the increased performance every 18 to 24 months. Today a typical processor chip contains billions of these transistors, and these transistors are the fundamental active elements of any processor, switching on and off to store the logical equivalent of zeros and ones representative of data and is how basic electronic functions are carried out.

Until recently, this increase in transistor density has been almost uniformly obtained by advances in the photolithographic processes used to create these structures on a chip, which has resulted in smaller and smaller features packed more and more closely together. Decreases in the size of transistors on a chip both increases the speed a chip can operate and the amount of data that can be stored while simultaneously resulting in a decrease in the manufacturing cost. To date, the most advanced chips have features as small as 65 nanometers. The next major milestone is a decrease in this feature size to 45 nanometers, but simply shrinking the feature size, which is a formidable task in itself, is not sufficient because at this scale crosstalk, or the undesirable leakage of electrical current from a transistor between parallel lines in a circuit, is considerable. This can cause signals that are supposed to represent a logical one flip to a zero and vice a versa, and can result in anything from inaccurate computations to data corruption.

Chipmakers including Intel, IBM and Texas Instruments are now taking measures to address this by replacing silicon and silicon dioxide, the materials that have been the backbone of the information age for over the last 40 years, with newer materials such as hafnium to help minimize this leakage of electrical current. Intel states that the adoption of this new material, along with a couple of others that have yet to be disclosed, will allow the company to double the number of processors while still occupying the same amount of space.(Greene, 2007a) This will permit future chip designers with the option of either boosting the number of processors per chip to make chips faster, or reducing the footprint of their current chips by squeezing the same chip designs into a smaller space and reducing their manufacturing costs.

The other major limitation in the determination of the size of features definable on a chip aside from the materials used is due to the lithography used to create features themselves. The tools used for lithography make use of a light source and a collection of lenses and mirrors along with a transparent mask to define patterns on a silicon wafter that will ultimately house the chip. This imprint defined by the light source and the mask permits different materials to be deposited onto the surface in different places through a series of chemical reactions, much like light forms images on unexposed film. The tool used to create these features currently has a price tag in the neighborhood of $15m.(Spooner, 2004)

The latest lithography tools planned for use by Intel uses lenses and filters along with a ultraviolet (UV) light source to define these features on a silicon wafer. Their newest light source which makes use of their EUV tool has a wavelength of only 13.5

nm, although their current processes use a light source with a wavelength of 193 nm but can produce features as small as 50 nm. This setup will be used until 2009, after which the newer light source will replace the current source to produce features as small as 32 nm.

The price tag of the facilities that house these tools increase drastically with every decrease in feature size. The latest plant designated for construction by Intel is located in China and will cost them some 2.5b USD and is expected to enter production in 2010.(Lemon, 2007)(infoworld) This plant won't even be considered 'state of the art' once it finally does enter production. Intel's 'fab32' facility, which is supposed to house the technology used to produce features that are 32 nm in size and will be located in Arizona, is slated to cost over 3b USD.(Jade, 2005)

As the cost continues to creep higher and higher, manufacturers seek out new technologies to aid in both keeping costs down while simultaneously allowing them to adhere closely to Moore's Law. Current toolsets will permit them to follow Moore's law for several more years, but engineers are increasingly understanding the need to switch to new materials and designs to allow these trends to continue into the future. In particular, manufactures are investing considerable research and development efforts into using nanotechnology to allow them to continue adhering to the trends that produce products and advances consumers have enjoyed for decades. Present-day research in the integration of new materials include efforts in growing carbon nanotubes (CNTs) and nanowires (NWs) directly onto silicon wafers.(Hwang et al., 2005) IBM has even turned to using self-assembled polymers to form hole-filled foams around on-chip

wiring.(McConnel, 2007) These foams are then later removed and a vacuum is left in place as the dielectric material insulating individual gates from one another, and preventing crosstalk. This technique allows chip speeds to be increased by an additional 35% or permits a decrease in the power requirements by 15%. (You can choose one or the other, but not both.)

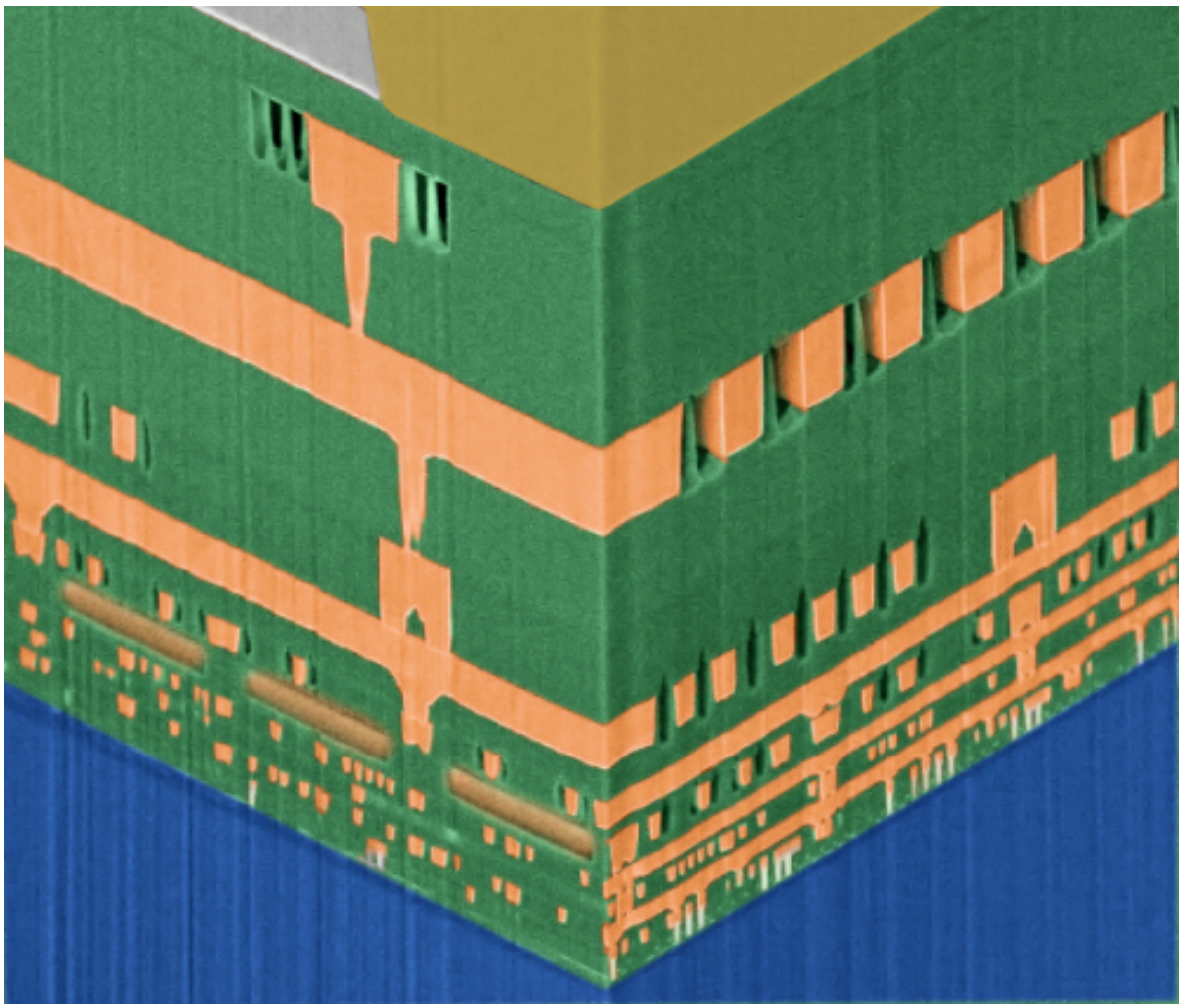

Figure 2.1: Chip made using IBM's air gap processing technology. Taken from ref (McConnel, 2007)

2.2 Integration of nanotechnology now and in the future

Although considerable efforts are now being placed into researching various areas for new materials and design adoption, the use of CMOS or CMOS-like transistors is expected to come to an as early as 2020 when transistors literally consist of only a few atoms, making it literally impossible to shrink them any further.(Kurzweil, 2000) Currently some of the most promising ideas that may eventually permit this level of miniaturization include spintronics(Engel and Loss, 2005) where electrons themselves store the state of a one or zero and materials that exhibit a change in the state of the phase of the material itself stores its contents(Agarwal, 2007). Optical technology using photonics is also shaping up to be another viable candidate, where the presence or absence of light itself stores the representative zero or one.(Barrelet et al., 2004; Sanders et al., 2006)

In the more foreseeable future, less radical paths are likely to be adopted. This is likely to be witnessed in the form of the integration of nanotechnology with current fabrication processes instead of complete and total replacement of current silicon-based technologies with nanotechnologies. Evidence of this can presently be seen in the integration of monodisperse nanocrystals with silicon wafer technology to produce non-volatile flash memories that use lower power and have higher write-erase life cycles. (Greene, 2007b)

The future, however, has others considering self-assembled systems composed of

DNA as possible structures that can eventually be integrated with current CMOS technology to extend its lifetime, and possibly even replace it entirely for certain applications. These structures look to the very core of biology to assemble predictable structures from the material that defines life itself due to the specificity of Watson-Crick base pairing.(Dwyer, 2003; Pease et al., 1994; Fu and Seeman, 1993; Cook et al., 2004) To date various structures and patterns have been self-assembled including some with spacings as small as 20 nm that are fully addressible.(Park et al., 2006) Computer architectures have also been proposed to make use of these structures and considerable headway has already been made in both preliminary theoretical designs and experimental implementation.(Kuekes et al., 2005; Han and Jonker, 2003; Cook et al., 2004) In order to function as useful computational devices, these architectures will require the design of fundamentally different active elements, or transistors.

2.3 Self-assembled DNA scaffolds

Self-assembled nanostructures composed of DNA were first formulated by Seeman in 1982.(Seeman, 1982) Structures formed from DNA generally make use of one or more repeating base units that are then self-assembled into larger, regularly patterned lattices. These base units include triangles(Chelyapov et al., 2004; Liu et al., 2003), squares(Park et al., 2006), psuedo-hexagons (Ding et al., 2004) , six-helix bundles(Mathieu et al., 2005), six-point stars(He et al., 2006) and parallelograms(Mao et al., 1999) – all of which have been used in the production of various 2d arrays of differing sizes, some

with single crystals being as large as 200 μm(He et al., 2006) . Rothemund has even managed to coerce single kilobase strands of DNA into intricate shapes and patterns by exploiting the self-assembly properties of DNA via what has been labeled 'DNA origami'.(Rothemund, 2006)

The general consensus to date supports the use of a multi-step fabrication process for the production of architectures produced by these type of self-assembly schemes. The assembly of the scaffolds themselves may or may not require multiple steps, depending on the complexity of the target structure and whether the route adopted for self-assembly makes use of a single assembly step or a hierarchal method. Useful products yielded from self-assembly will require the attachment of other types of materials to specific points on the lattices. This is evident in the preliminary architectures produced by several groups that produce the scaffolds first followed by the attachment of nanoparticles or other similarly sized objects such as viruses(Zhang et al., 2006a; Park et al., 2006; Sharma et al., 2006). Ultimately, these nanoparticles will likely be replaced by more useful structures, loosely known as 'nanowires', in order to begin mimicking the circuits produced by lithography today.

2.4 Nanowire fabrication

Some of the very first nanostructures that are now universally labeled as 'nanowires' were controllably produced by Possin and reported on in 1970.(Possin, 1970) His method involved the use of a thin sheet of mica filled with small holes having dimen-

sions roughly 40 nm wide and 15 μm long. This method helped lay the groundwork for what would later become known as templated nanowire deposition which involves using a sacrificial template to confine one dimension of the nanowires while the other dimension (the length) is variable and determined by the nanowire growth/deposition time. The template method is still widely used today (Kline et al., 2006; Riveros et al., 2005; Nicewarner-Pena et al., 2001) but mica has generally been replaced by anodic aluminum oxide (AAO) templates(Nielsch et al., 2001; Schonenberger et al., 1997), polycarbonate templates(Schonenberger et al., 1997) and in some instances even composite or silica based templates(Lu et al., 2004). Template based methods (and in particular nanowires grown in AAO templates) have several advantages over other nanowire fabrication methods including tight control over the diameters of the nanowires and as it will be demonstrated later, control over the location of functional groups on the surfaces of template grown nanowires. Nanowires capable of being produced inside of templates include both conducting(Yu et al., 1997) and semiconducting(Zheng et al., 2001) structures, and the template method has even been used to grow CNTs(Hwang et al., 2005).

Other methods employed in the fabrication of nanowires include solution based routes which don't require the presence of a negative template at all. In some instances, DNA itself has even been use as a positive template for the attachment of small nanoparticles including nanoparticles made of platinum(Gill et al., 2000), silver(Braun et al., 1998), gold (Patolsky et al., 2002), palladium(Deng and Mao, 2003) and copper(Monson and Woolley, 2003) in order to produce nanowires. Structures formed by

this method usually have diameters of several tens of nanometers, and the variation in the diameter over the length of the nanowire is usually non-uniform and non-negligible. Vapor deposition methods (CVD, VLS) may also used to produce nanowires with diameters consistently less than 100 nm. Nanowires produced by vapor methods include GaO (Song et al., 2004), germanium(Greytak et al., 2004) and ZnO(Song et al., 2005) which have all been produced by VLS, and ZnO(Ng et al., 2004), (Fan et al., 2004) produced by CVD. Thermal evaporation has even been used to produce nanowires without a template.(Byon et al., 2005) Core-shell and vertical gate structures have been produced by vapor methods as well.(Ng et al., 2004),(Lauhon et al., 2002) Other methods include routes which make use of surfactants(Grebinski et al., 2004) and routes that are surfactant–free(Shao et al., 2004) to produce both straight and branched nanowire structures.

2.5 Determination of electrical properties of semiconducting nanowires

The electrical properties of individual nanowires have undergone significant study over the past several years and it has been found that characteristics such as majority carrier mobility of these structures almost always varies drastically from bulk values due to large differences in surface to volume ratios of the bulk materials and the quasi-one-dimensional equivalent shapes that are nanowires. Researchers usually attribute differences in parameters such as the electron mobility to redistribution of the electron

density in the conduction channel to the surface of these nanostructures due to applied biases, where an increase in the scattering probability results in a degradation of the electron mobility.(Kolmakov and Moskovits, 2004) For instance, the bulk value for the majority carrier mobility of CdS is 340.0 cm^2 V^{-1} s^{-1} but the mobility reported in a nanowire with a diameter on the order of 100 nm is an order of magnitude lower at 32.20 cm^2 V^{-1} s^{-1}.(Zhang et al., 2006b) As such, it is generally true that observations of electrical properties made for bulk materials don't readily apply to nanoscale structures. One method of extracting properties such as the bulk mobility from these structures involves depositing already constructed nanowires onto a silicon/silicon oxide substrate from solution and forming contacts to individual nanowires via lithography.(Williams et al., 2003) The nanowires can then be individually addressed and its conductance can be modulated by using the substrate as a global gate.(Huang et al., 2001) Local gates can also be defined lithographically as a top(Lauhon et al., 2002) or lateral gate(Clement et al., 2002) or through other nanowires themselves.(Huang et al., 2001) The conductivity of individual nanowires has also been gated through the generation of a photocurrent by illuminating optoelectronic structures with light.(Pena et al., 2002) The use of any of these geometries results in modulation of the semiconducting channel of these nanowires and the electrical properties can be investigated accordingly and parameters can be extracted including the transconductance, carrier mobility, and number of donors. In addition, there have been several studies conducted on bundles of nanowires in order to observe the electrical properties of these structures as well.(Pena et al., 2002)(Klein et al., 1993)

Electrical characterization of nanoscale structures has also been performed through other methods, although these techniques tend to be used less than conventional lithography methods due to the amount of information any one technique is generally capable of yielding. For example, uv-vis spectra are often collected for nanostructures in order to determine the optical bandgap since the absorption peak is dependent on the bandgap energy of the underlying structure and for smaller structures on quantum confinement.(Kwak et al., 2007) Electrochemical impedance spectroscopy (EIS)(Beach et al., 2003) is a method that can detect the capacitance of the depletion region of a semiconductor by using an electrochemical cell and a suitable electrolyte such as a pH buffer. An equivalent circuit is selected after collecting the data, and the spectroscopy data can be used to determine the values of various components of the circuit. The capacitance can be extracted, and this can be used to construct a Mott–Schottky plot in order to determine the carrier density of the semiconductor under investigation. As such, EIS can give information about band-edge potentials.(Beach et al., 2003; Mora-Sero et al., 2006; Bisquert, 2008) Additionally, photocurrent measurements can also provide information about the band-edge potential of the material, and the material type can also be determined by monitoring anodic or cathodic currents.(Wang and Tao, 2007) While each of these methods can yield valuable information about the structures under investigation, no single method is capable of providing the amount of information that can be obtained from electrical measurements that yield 'standard' current–voltage (I–V) curves. The information that can be extracted from these data include but are not necessarily limited to the transconductance, majority carrier mobility, material

type (n–type or p–type), gate threshold voltage, majority carrier concentration and information about the contact barrier height established between the metal electrodes and semiconductor nanowire.

2.6 Nanowire mechanics

In comparison to the amount of information available on the electrical properties of nanostructures, the information available on the mechanical nature of these structures is relatively scarce. The tool of choice for these types of investigations is typically the atomic force microscope (AFM) since it allows direct manipulation of the structures of interest. Vertically aligned nanowires of ZnO have been investigated with this method in order to determine the elastic modulus(Song et al., 2005) as well as the fracture strength and Young's modulus(Hoffmann et al., 2007). Mechanical measurements have also been performed on nanowires anchored down to a substrate and suspended horizontally across predefined trenches.(Wu et al., 2005)(Wu et al., 2006) The Young's modulus and yield strength were both determined for structures in this configuration, and the Young's modulus was found to be independent of the nanowire diameter and the speed at which the cantilever performed the manipulation on the nanowire. Other groups have used SEM(Yu et al., 2005)(Dikin et al., 2003) and TEM(Wang et al., 2002; Wang, 2003; Wang et al., 2001) instruments to determine the bending modulus of quasi–one–dimensional nanostructures via electron beam and field induced actuation. Thermally driven mechanical deflection of nanowires has also been observed.(Ikuno et al., 2005)

Chapter 3

Selective Functionalization of Nanowires

3.1 Nanowire construction overview

Over the past few years, a large number of nanoscale devices have presented themselves as candidates to serve as fundamental elements in both future nanoscale systems and computational devices. These candidates have included carbon nanotubes (Bachtold et al., 2001) and nanowires fabricated from various materials.(Fan et al., 2004; Kovtyukhova et al., 2004; Byon et al., 2005) Nanowires are one type of several quasi-one-dimensional (Q1D) structures that have large aspect ratios and can be produced from porous alumina (PA) templates with diameters within the range of one to several hundred nanometers. Various methods are presently in use that allows for the fabrication of these structures including chemical vapor deposition (Greytak et al., 2004), solution-based methods(Mitamura et al., 2007), lithography(Koops et al., 1995), step-edge deposition(Menke et al., 2004),DNA based deposition(Keren et al., 2004) and

template based deposition.(Pena et al., 2002; Nicewarner-Pena et al., 2001)

The template fabrication method allows for the diameters of the nanowires to be defined by the size of the pores in the template. Because various sets of parameters including the anodization voltage, the electrolyte temperature and the anodization acid used will produce different pore sizes in these templates, the resulting nanowires have diameters ranging from several hundred nanometers down to 8 nm or less.(Wade and Wegrowe, 2005) Thus, the size and size distribution of the nanowires are directly determined by the size and the size distribution of the pores of the template. The length of the nanowires produced in the template is determined by the amount of time the material constituting the nanowires is deposited and also by the rate of deposition. Additionally, the material deposited is adjustable as well. This feature is unique to the template based deposition that is not easily controllable in methods that involve solution based growth and therefore template deposited nanowires can be produced with arbitrarily varying material composition along the length of the nanowire simply by varying the composition of the plating bath. Nanowires constructed from templates are generally formed in templates one or more of three different materials: polycarbonate track-etched membranes (PCTE), anodic aluminum oxide (AAO) which are also known as porous alumina (PA) templates , or the so-called SBA-15 materials. Each has its benefits which will briefly be outlined here.

PCTE membranes are flexible membranes that have nano and micro-sized pores that have been formed through a technique known as the 'track etching'. This method involves irradiating polycarbonate foils in an accelerator with heavy ions, causing cylin-

drical tracks to be left in the irradiated foil due to energy loss of the ions as they interact with the foil.(Schuchert et al., 2003) These tracks can then be widened by chemical etching, and can produce uniform pores of arbitrary sizes as long as the energy of the heavy ions bombarding the PCTE membrane is sufficient. The main benefits of these templates is their flexibility, which allows for easy handling, and the ability to roughly control the average spacing between pores (c.a. AAO membranes which have pores that are packed a lot more closely). The main disadvantages of these templates includes their inability to withstand high processing temperatures, the random distribution of the placement of the pores on the surface, and the non-parallel orientation of the pores with respect to each other which results in some pores crossing with others, and causes any material deposited within these joined pores to appear as one misshaped nanowire instead of two separate entities.

AAO templates are ceramic materials with a closely packed and hexagonally ordered pore structure. The pores can have sizes ranging from 7 or 8 nanometers up to a couple of hundred.(Wade and Wegrowe, 2005) These templates are formed by the electrochemical anodization of aluminum foil in acidic conditions. Typically, a piece of polished, high-purity aluminum foil is placed as one electrode in an anodization bath while in the presence of another electrode. A voltage is set between the two electrodes, and the metallic aluminum foil is slowly converted into a porous aluminum oxide. Both the composition and the temperature of the bath determine the size of the pores formed, and the thickness of the aluminum oxide sheet is determined by the anodization time. One of two options is typically taken after the formation of the aluminum oxide thin

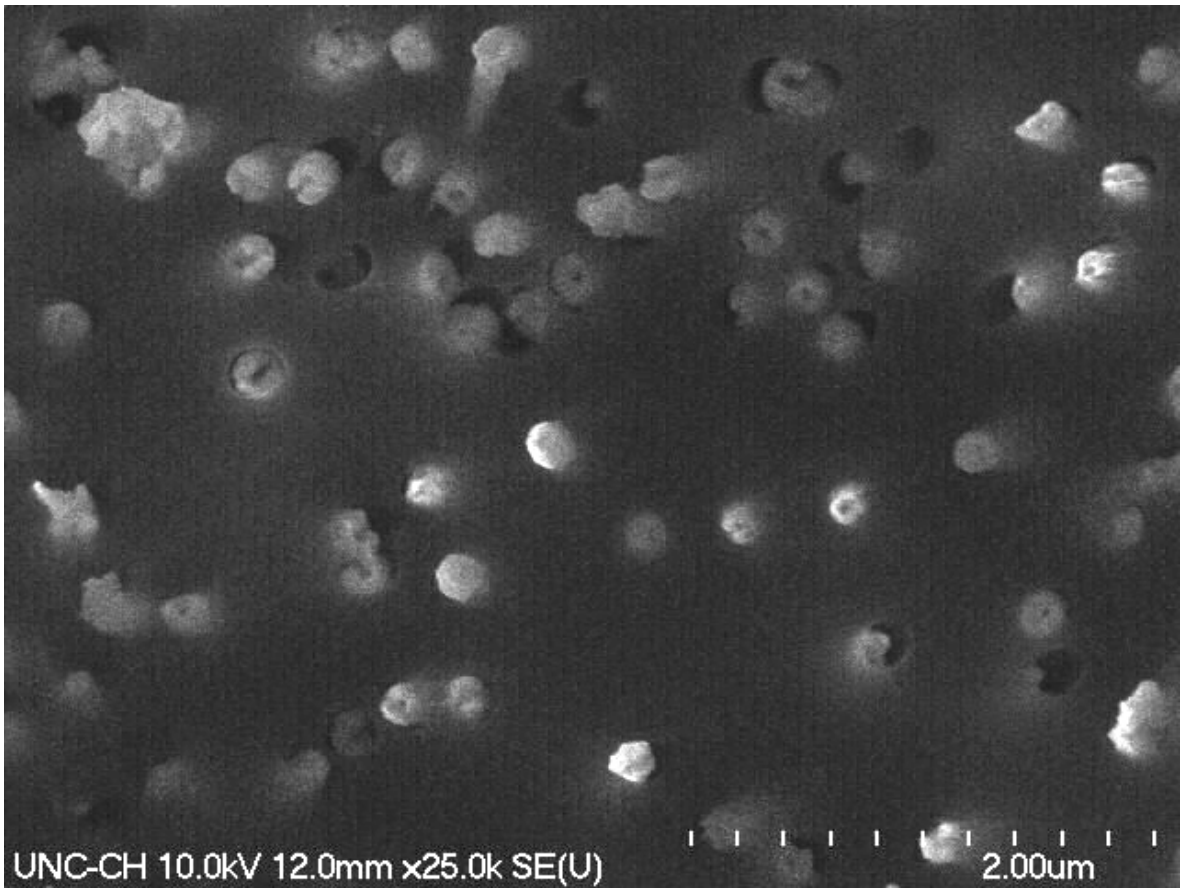

Figure 3.1: Top-down view of 200 nm pore PCTE membrane with embedded Au nanotubes.

film, depending on whether an aluminum oxide template is preferred with through-holes (like the PCTE membranes described above) or whether one wishes to leave the template attached to the original aluminum foil support. Nanowires can be produced in both of these templates in either case.

A third type of template that is relatively new but is gaining much attention are the so-called SBA-15 templates. These mesoporous materials are a special class of nano-materials with ordered nanopores with pore sizes between 3 and 30 nm.(Yang et al., 2003) They posses high thermal stability and are expected to be useful in applications

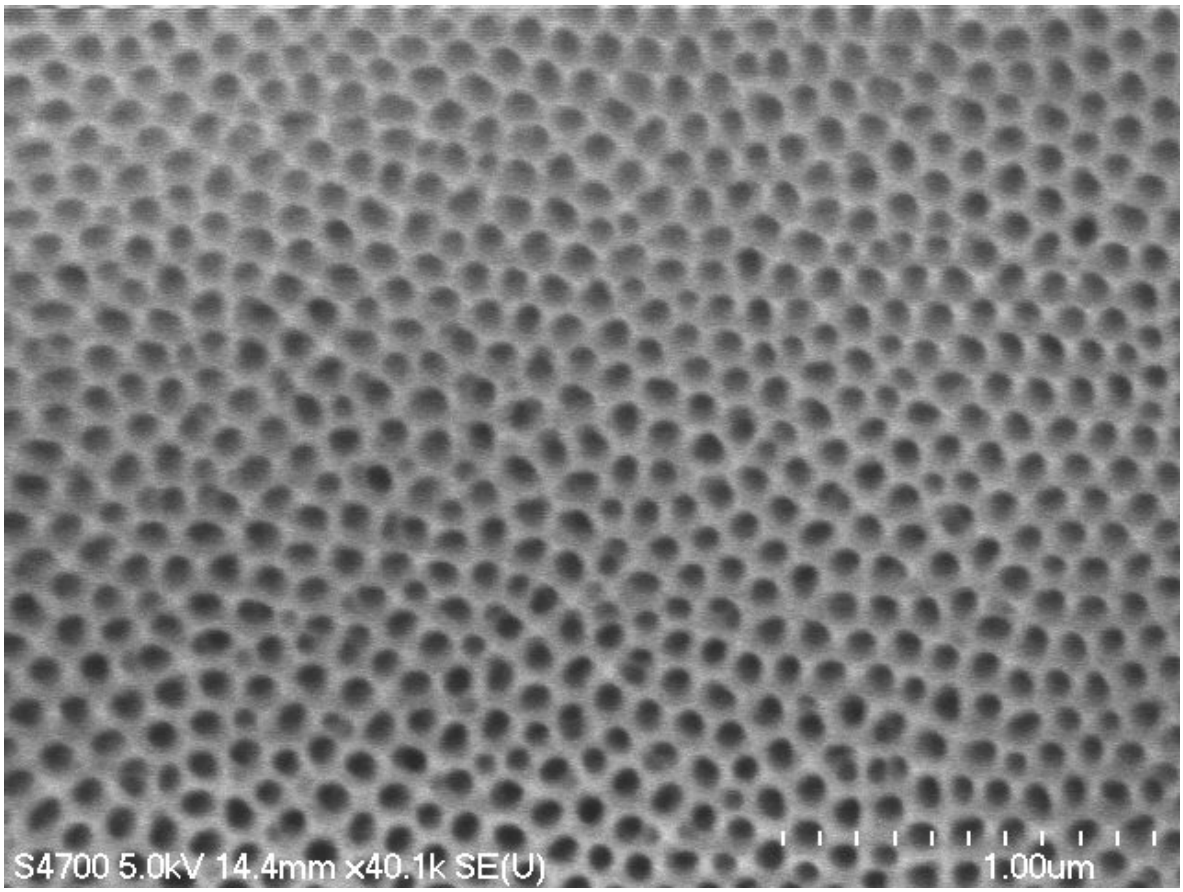

Figure 3.2: AAO template with 80 nm pores.

requiring high-density but separated nanowire arrays.(Lu et al., 2004) These block copolymer-silica structures are formed through a sol-gel method, and because this material faithfully replicates the vessel the reaction is carried out in, different templates can be used for the production of this material including AAO templates. Figure 3.4 contains a 4.8 cm long by 2.1 cm wide by 0.2 cm sample of the ordered transparent mesostructured block copolymer-silica that has been removed from its mold, and Figure 3.5 contains the block copolymer that has taken the shape of 200 nm nanowires as the pores of AAO templates were used for the mold.

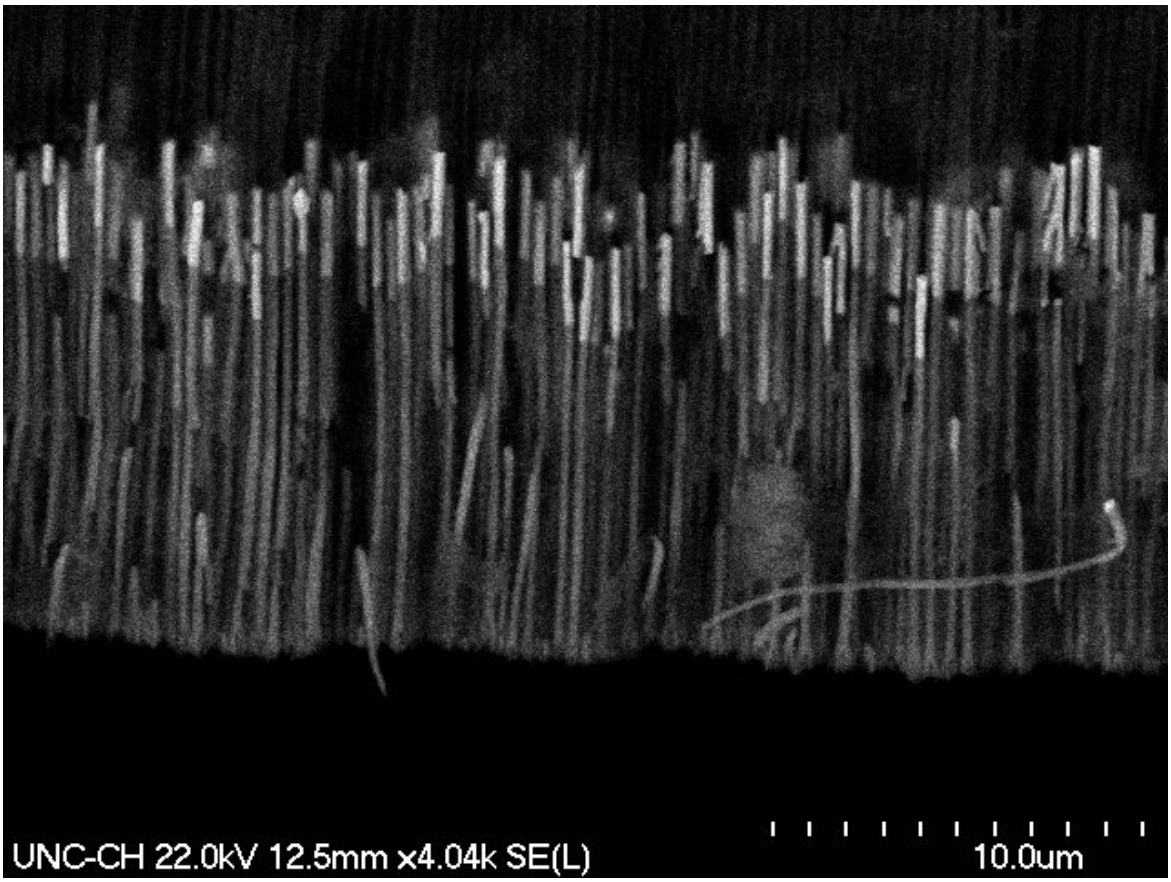

Figure 3.3: Profile view of 200 nm Cu nanowires with Au tips still embedded in an AAO template.

Unless otherwise stated, the nanowires that are referenced throughout this dissertation are constructed from commercial AAO templates and were fabricated via electrochemical deposition techniques. Specifically, the AAO templates used here were primarily the Anodisc variety obtained from Whatman, Inc. and contained 200 nm pores. It is important to note that although the rated pore sizes of the AAO template is 200 nm, the actual pore sizes tyically range between 200 and 350 nm depending on the individual template. The sizes of the pores of the templates used here refer to the rated values provided by the manufacturer, and not the actual sizes of the pores

Figure 3.4: Photograph of an ordered transparent mesostructured block copolymer-silica monolith. Taken from (Yang et al., 2003)

themselves. Although this manufacturer also sells AAO templates with pore sizes of 100 nm and 20 nm, it was discovered that the diameters of the pores were not uniform throughout the 60 μm thickness of the entire template. Figure 3.6 is an SEM micrograph of one of the 20 nm Anodisc templates that has been broken into two in order to show the non-constant diameter of the pores. The pores start out with diameters of 20 nm (upper portion of image), but quickly changes to larger dimensions and the remainder of the length of the pores assumes a pore size comparable to the 200 nm rated pores. Because the actual length of the pore with a diameter of 20 nm is less than

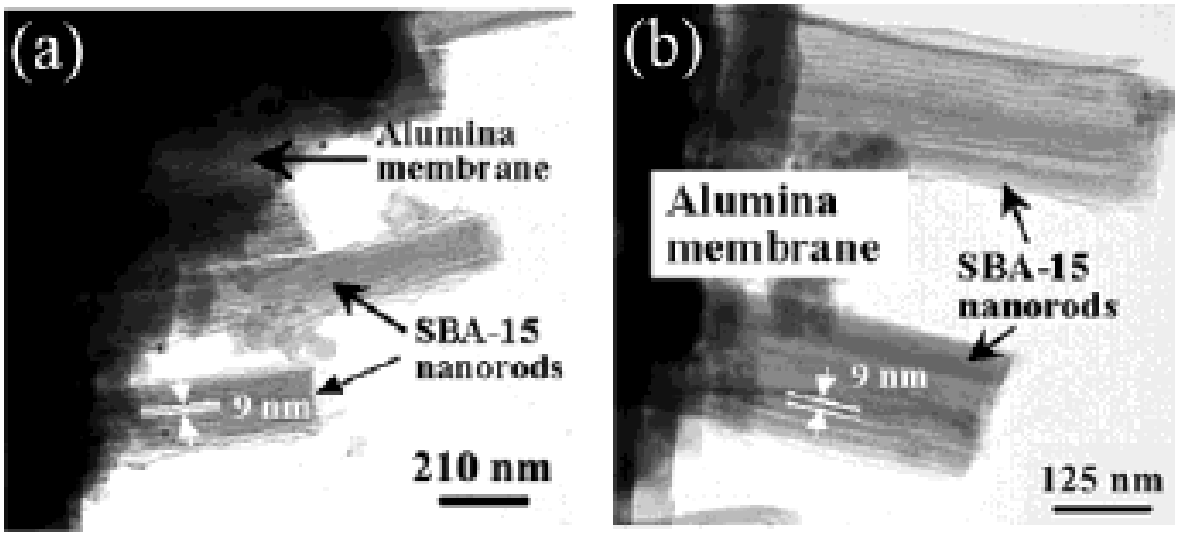

Figure 3.5: TEM images of an AAO template with SBA-15 inside the pores. Taken from (Lu et al., 2004)

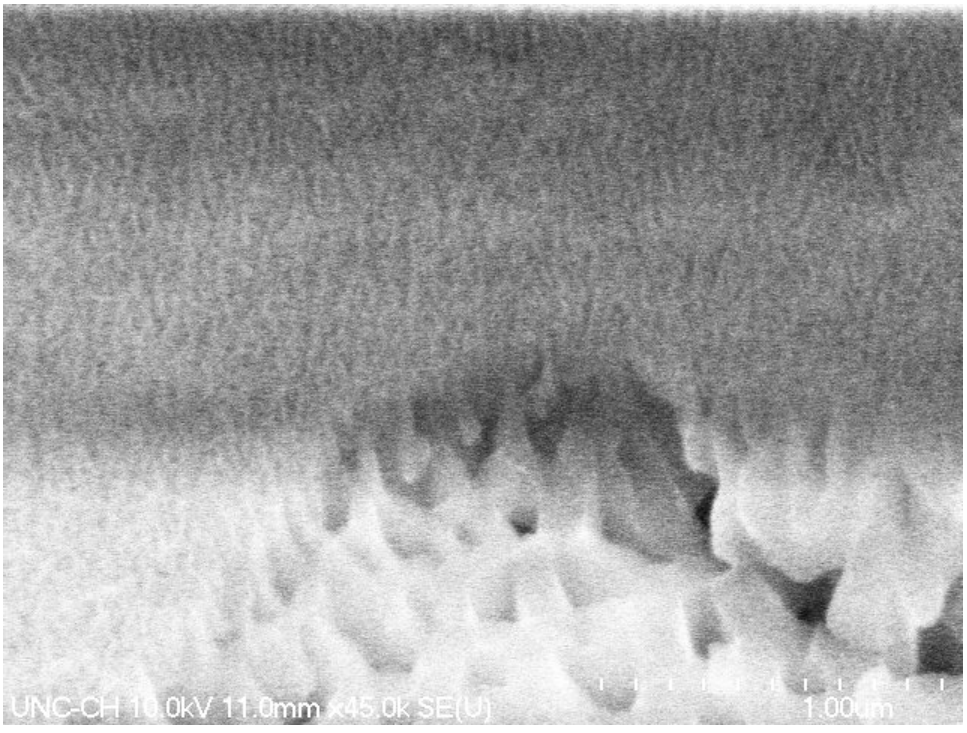

Figure 3.6: Tilt-stage view of a 20 nm AAO template broken in half. The 200 nm pores beneath the surface is evident in this picture. Scale bar is 1 μm.

a few hundred nanometers, these templates were not usable for depositing nanowires for the majority of the experiments performed here and resulted in considerable effort being devoted to fabricating templates of these dimensions in house. Fortunately, a different manufacturer, Synkera Technologies, began producing their own templates with similar macroscopic dimensions to address this very problem, and templates with pores as small as 13 nm have been routinely acquired from them for experiments conducted for the growth of nanowires for the attachment to DNA lattices.

3.2 Electroless deposition of single material nanowires

3.2.1 Introduction

The electroless deposition of metal onto a surface involves the reduction of a metal ions in solution using a chemical reducing agent. Because the substrate does not have to be conductive, one advantage of this method over electrochemical methods is that the substrates often require no special preparation for conductivity purposes before use. The main requirement of this method, however, is that the transfer of electrons from the reducing agent to the metallic ions in solution is slow, which prevents the bulk reduction of the metal in solution all at once. Additionally, if a catalyst is placed on the surface of substrate of interest, reduction will preferentially take place here and not on other surfaces accessible to the reduction medium.

The electroless chemistry used in this paper is a slight modification of the method developed by Menon and Martin (MENON and MARTIN, 1995). PCTE membranes

are often coated with poly(vinylpyrrolidone) (PVP) in order to promote wetting of the pores when immersed in aqueous solvents (these membranes are intended for use as filtration devices, after all). This deposition technique involves using a sensitizer (Sn^{2+}) that binds to PVP in order to coat the surface of the membrane with a metal since PVP contains metal-complexing amine and and carbonyl groups. The surface is then activated with ammoniacal silver nitrate which causes Sn(II) to be oxidized to Sn(IV), and the Ag^{+} is reduced to elemental Ag and coats the surface of the membrane with nanoscopic particles of Ag. The membrane is then placed in a plating bath of Au, which causes the Ag particles to be galvanically replaced with Au particles since Au is a more noble metal. These particles then act as catalytic sites for the oxidation of formaldehyde and the subsequent reduction of Au(I) to Au(0).

As far as is known, this work contains the first instance of 200 nm Au nanowires formed in PCTE membranes based on electroless chemistry (see Figure 3.7). The modifications made to Menon and Martin's procedure was necessary due to the formation of nanotubes instead of nanowires. Namely, if the concentration of the Au plating bath is insufficient for filling all of the pores of the membrane nanotubes will form instead of nanowires since the deposition of Au proceeds beginning at the surface of the pores in the membrane. The inner diameter of these tubes can be controlled either by the amount of Au present in the plating solution or by limiting the amount of time the plating reaction is allowed to proceed, as is evident in figures 5.1 and 3.7.

3.2.1.1 Experimental

The fabrication of 200 nm nanowires in PCTE membranes is initiated with the preparation of the Sn sensitizer solution, which was composed of 0.026M $SnCl_2$ and 0.07M trifluroacetic acid, with a solvent of 50/50 methanol/water. The PCTE membrane was immersed in this solution for 3 min, and the membrane was then rinsed with 3 times with large quantities of methanol. The Sn^{2+} coated membrane was then activated with a 0.029M solution of ammoniacal silver nitrate. The membrane was then rinsed in 2 times with copious quantities of methanol and then placed in distilled water. For the final step, the Ag coated membrane was placed in a reduction bath containing 1.2 x 10^{-1}M $Na_3Au(SO_3)_2$ (the commercial plating solution of Oromerse Part B diluted with distilled water), 0.127 M Na_2SO_3 and 0.625 M formaldehyde which had been chilled to ˜2°C before adding the formaldehyde as its addition will cause the deposition reaction to commence immediately. The plating of Au onto the PCTE membrane proceeded overnight (typically about 18 - 24 hours) and was removed from the plating solution and rinsed with water and methanol before being air dried under a stream of nitrogen.

Menon and Martin were able to gain access to the nanowires formed in the PCTE membranes by applying tape to the surface of the membrane and then removing it, causing the thin film of metal formed on the surface of the membrane to be removed with the tape and providing access to the nanowires themselves. This was applicable for their samples since the amount of metal deposited on the surfaces of their templates was a minimum of 5 and 30 nm in thickness. The nanowires produced here had diameters in

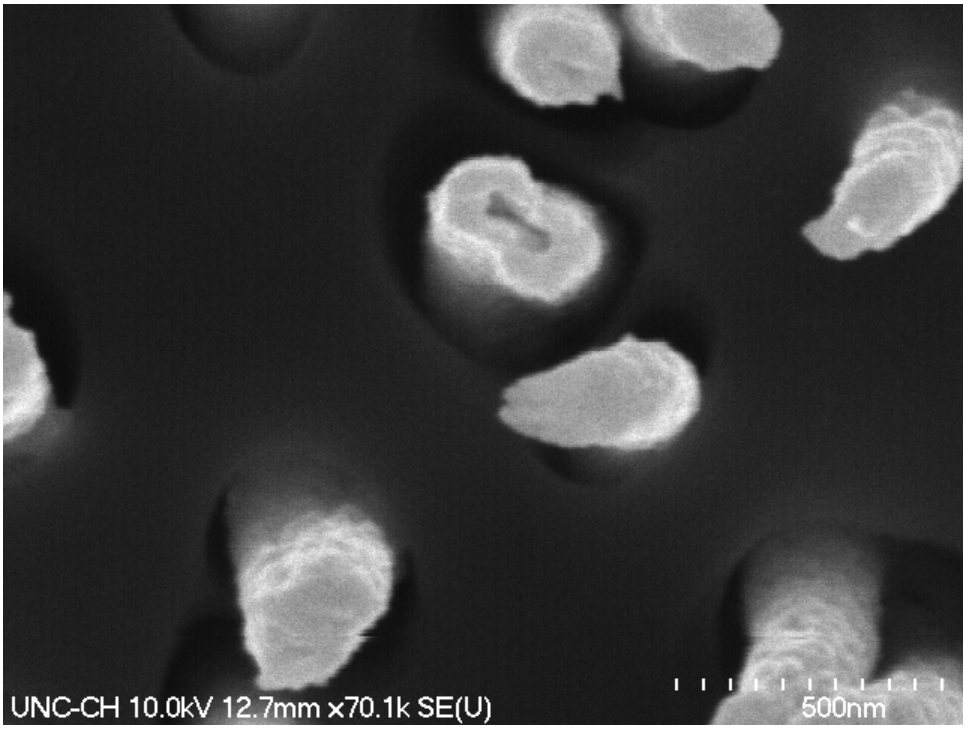

Figure 3.7: 200 nm Au nanowires formed by electroless deposition. Nanowires with oblong tips result from removing the gold layer coating the entire surface of the membrane in order to gain access to the nanowires themselves.

excess of 100 nm, and lengths on the order of 10 μm, which is defined by the thickness of the template. Any attempts in removing the layer of metal deposited on the surface of the membrane resulted in only a thin surface layer of the metal being removed. Repeated applications of the tape would eventually cause the membrane itself to tear.

3.2.2 Results and discussion

Due to the thickness of the metal layer, the most straightforward method of gaining access to the nanowires was to apply ample pressure to the surface of the membrane while wiping it off with a Kimwipe, which caused a visible color change on the surface of

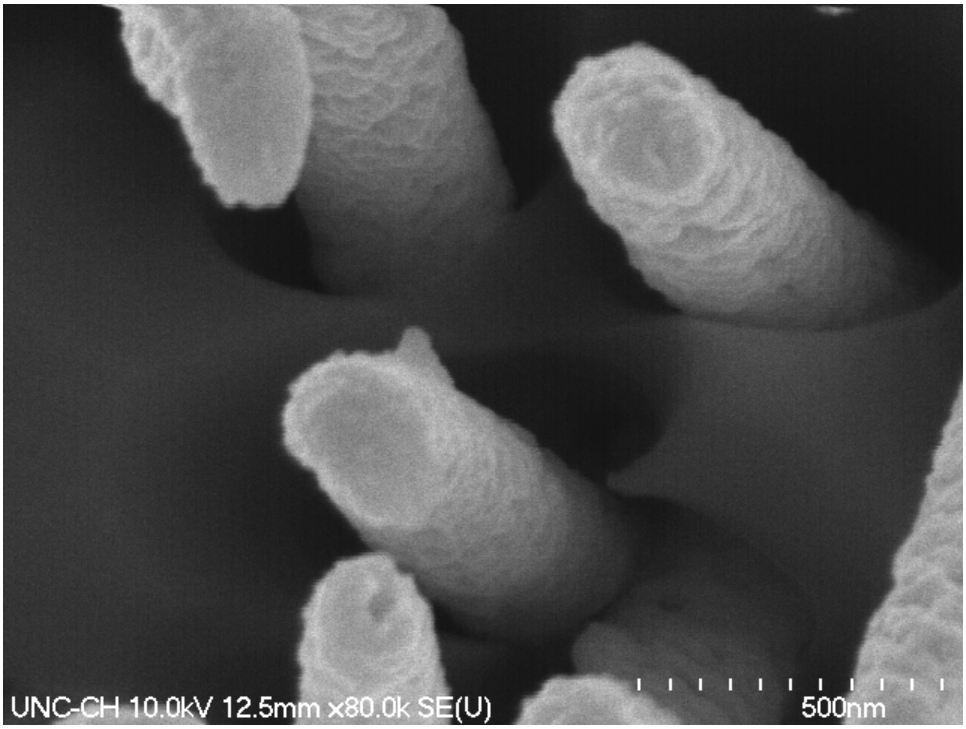

Figure 3.8: High magnification SEM of 200 nm Au nanowires showing the amount of surface roughness.

the membrane as the metal layer was removed. Unfortunately, the amount of pressure applied to the surface of the membrane while wiping also induces large amounts of sheer stress on the membrane itself, and causes the nanowires within the membrane to undergo sheer stress as well. This results in bent tips at the ends of the nanowires as seen as elongated tips appearing as ellipsoids on some of the ends of the nanowires as seen in Figure 3.7, and immediately makes them less usable if quasi one-dimensional structures are desired as this process introduces an asymmetry into the physical structure of the nanowire.

Additionally, Figure 3.8 clearly shows the amount of surface roughness present on the outer surfaces of the nanowires, even though other groups have reported that the

walls of the PCTE membrane pores themselves are relatively smooth.(Nasirpouri et al., 2007) The roughness present in the nanowires here likely results from the rate that the reaction occurs during the initial moments of the electroless deposition process. A change in the kinetics of the reaction such that the reaction is slowed down may allow for the formation of smoother surfaces of the deposited nanowires.

The nanowires seen in both Figure 3.7 and 3.8 have had a portion of the surface of the PCTE membrane removed by ozone plasma etching,(Yu et al., 2003) which was achieved by placing the PCTE membrane into the chamber of an oxygen plasma cleaner. This process of separating the template from the nanowires is relatively slow, requiring 15 minutes of etching at 100W to remove a couple of microns of the template-based on previously conducted experiments. Figure 3.7 also shows two separate pores that are in close enough proximity that what should have been individual nanowires have coalesced into one; a problem that is common with these types of porous membranes unless the density of the tracks created by heavy ion bombardment is sufficiently low enough that the probability of two ions creating two separate tracks in close proximity is sufficiently small. This however significantly decreases the density of the number of nanowires that can be created, and therefore is not desirable for applications that wish to make use of massively parallel device construction routines.

In terms of cost, the electroless deposition route is also somewhat wasteful, as a significant amount of the metal being reduced is also deposited non-specifically on the outer surfaces of the PCTE membrane as well as on the surface of the vessel the reaction is carried out in. These shortcomings, along with the inability to control the length of

the nanowires produced in the PCTE membranes (which is determined by the thickness of the membrane itself) resulted in alternate methods to be sought out.

3.3 Electrochemical deposition of single-material and heterostructured nanowires

3.3.1 Introduction

Electrochemical deposition is the general process describing the reduction of metal or semi-metal ions from solution onto a conducting substrate. The general conditions required for this to occur includes a solution of the proper composition (material, concentration, pH, etc.) and a potential of the appropriate magnitude applied between two conducting electrodes in solution, one of which being the electrode that is to be the target for the deposition of metal. The general reaction for this process is

$$\mathrm{M}^{\mathrm{z}+} + \mathrm{ze}^{-} \longleftrightarrow \mathrm{M}(s). \tag{3.1}$$

When the necessary conditions are satisfied, namely when the proper potential is applied between the two electrodes in solution and the proper pH conditions exist, the result is a metallic or semi-metallic precipitate formed on the cathode (i.e. working electrode) of the experimental setup. Thus the ions of interest in solution can be reduced from solution onto the electrode in the presence of a sufficient potential between the two electrodes. This potential requirement is satisfied when the potential difference

between the working electrode and the solution is more negative than the potential difference at equilibrium conditions U_{eq} when no net reaction occurs. The opposite is true as well, and when the potential difference between the working electrode and the plating solution is larger than U_{eq}, deposited metal will be dissolved since the ionic form is favorable.

A quick assessment of the deposition conditions that will permit the reduction of the material of interest from solution can be determined from a Pourbaix diagram. These diagrams are mappings of pH-U space that shows which phases are thermodynamically stable for a pH and potential of interest. Ion boundaries are represented by lines indicating the stable phase, and these diagrams can be read much like phase diagrams. Figures 3.9, 3.10, and 3.11 contain the Pourbaix diagrams for Ag, Au and Cd respectively; materials that were all used in the construction of the nanowires to be discussed in this section. These diagrams show that the ionic phase of these metals are only stable over certain pH and potential ranges. For example, from Figure 3.10 we can see that at a pH of 6 gold oxide forms at potentials above 1.2 V. When we also consider the boundary between where water is stable and the liberation of hydrogen occurs in Figure 3.12, we see that hydrogen evolution occurs over most of the potential range where Au deposition also takes place.

The pourbaix diagrams included here are only rough indicators of the conditions required for the successful reduction of metallic ions onto an electrode. Optimization of these conditions requires a cyclic voltammogram (CV) to be performed for each deposition bath of interest, as this presents a more detailed view and understanding

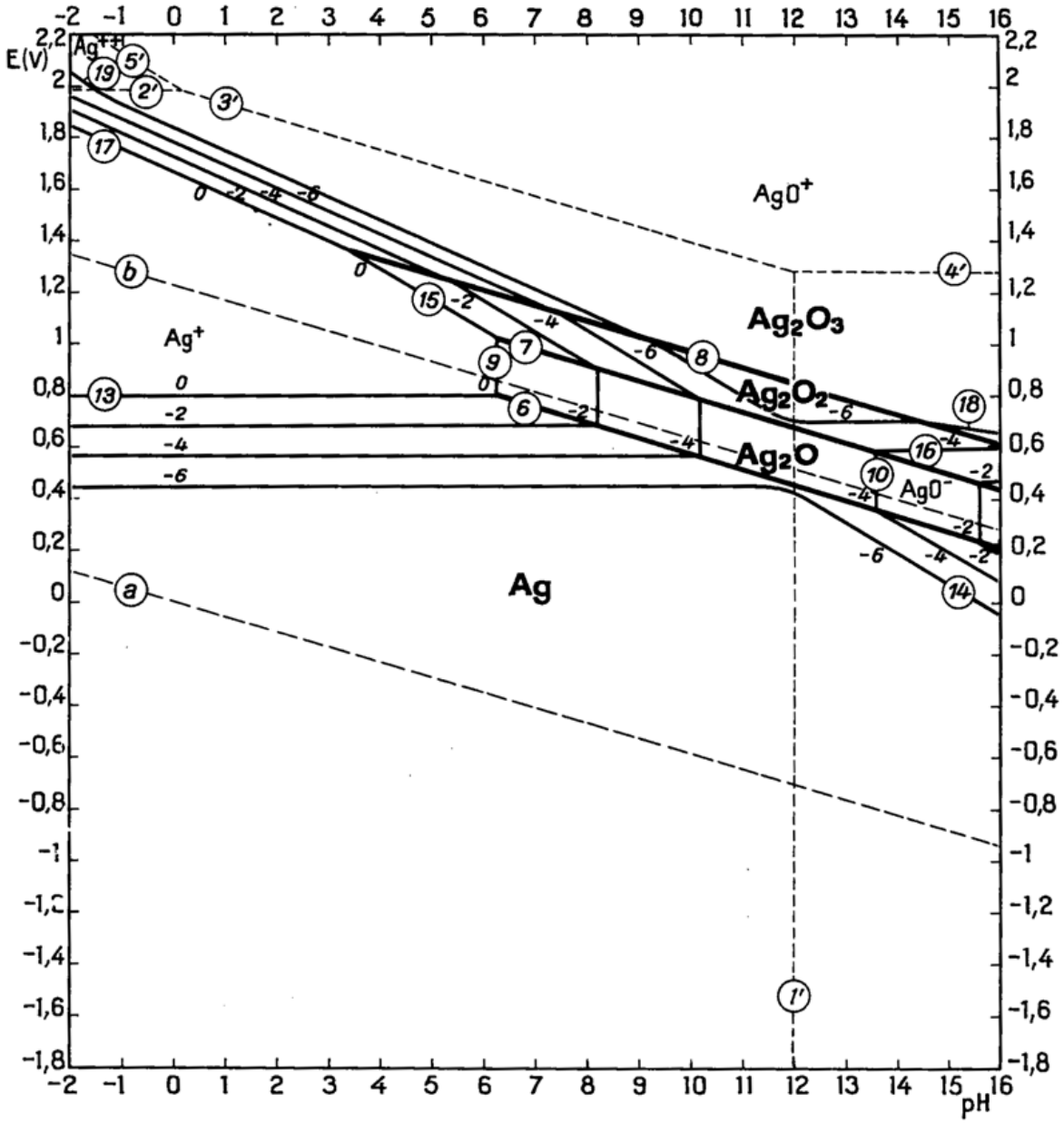

Figure 3.9: Pourbaix diagram for the system silver-water at 25°C.

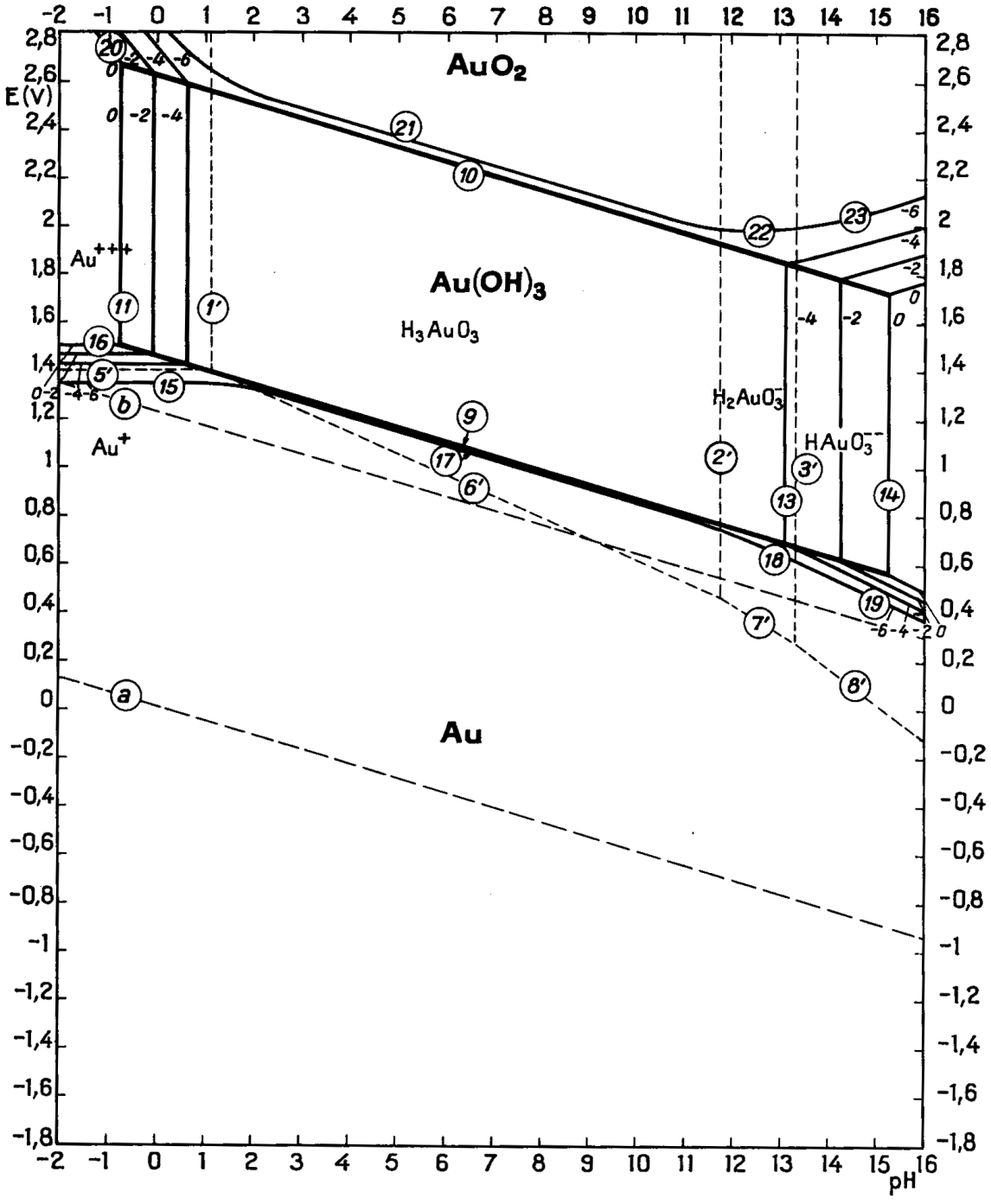

Figure 3.10: Pourbaix diagram for the system gold-water at 25°C.

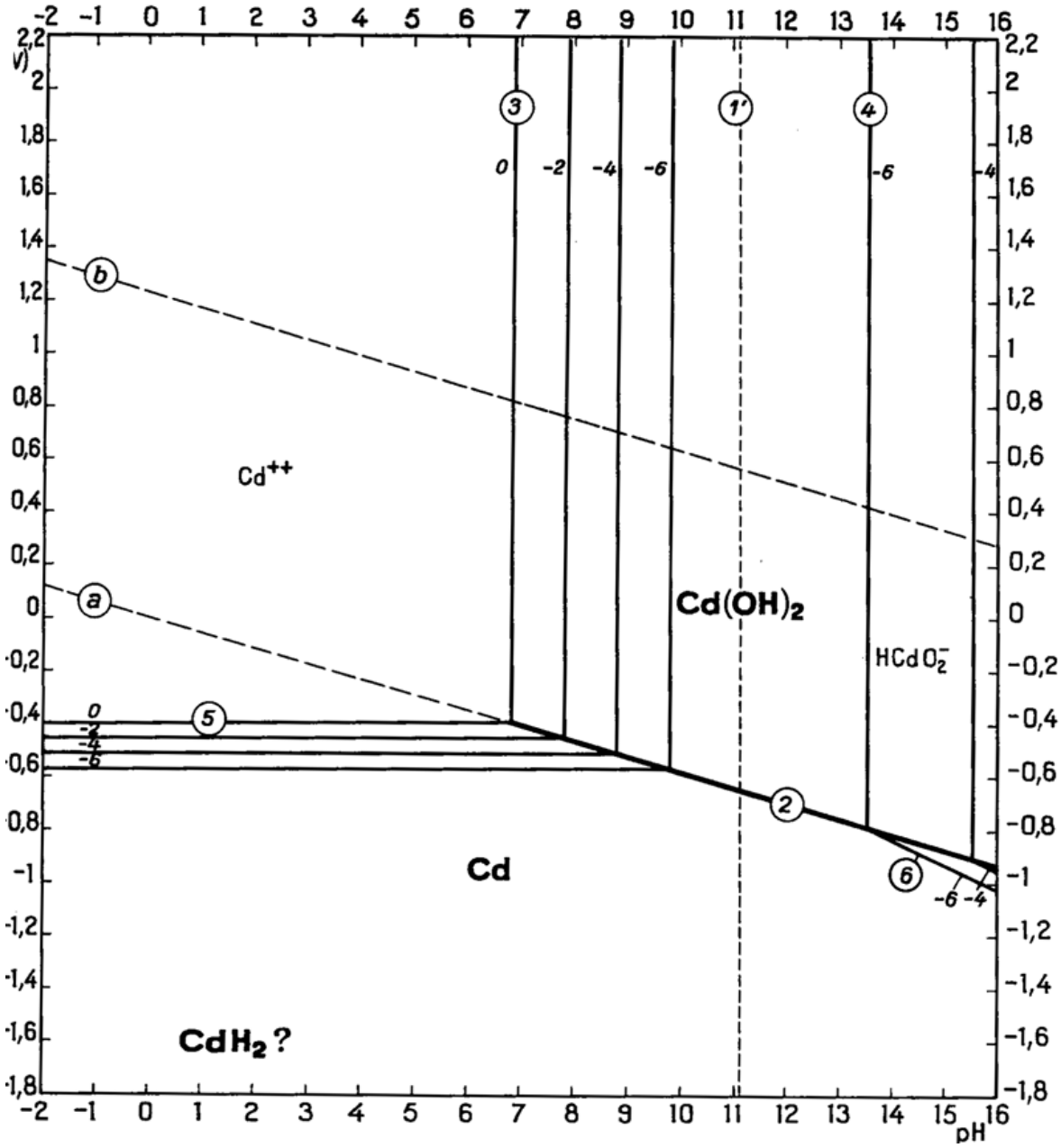

Figure 3.11: Pourbaix diagram for the system cadmium-water at 25°C.

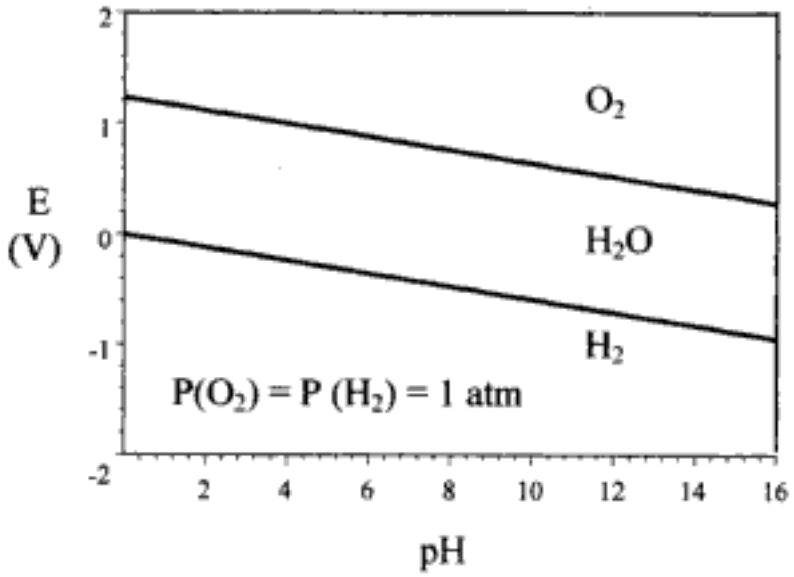

Figure 3.12: Pourbaix diagram for the system cadmium-water at 25°C.

of the kinetics of the system during electrodeposition. As is evident in figure 3.13, an increase in electrodeposition current occurs as a more negative potential is applied. At sufficiently large current densities, the reaction becomes rate limited by diffusion. In aqueous solutions, hydrogen evolution is also a byproduct of increasingly negative potentials. The local minima of this reduction peak denotes where deposition of the electroactive species in solution begins, and any value at this peak or lower may be chosen for electrodeposition as long as hydrogen evolution is considered when depositing at more negative potentials.

All of the CVs in Figures 3.13 – 3.15 were collected using 200 nm AAO templates. Analysis of these CVs allows one to determine a range of appropriate potentials to use for the deposition of the metal of interest from solution. For the silver and gold ion containing baths, a potential of -1 V was chosen for the deposition of nanowires. For

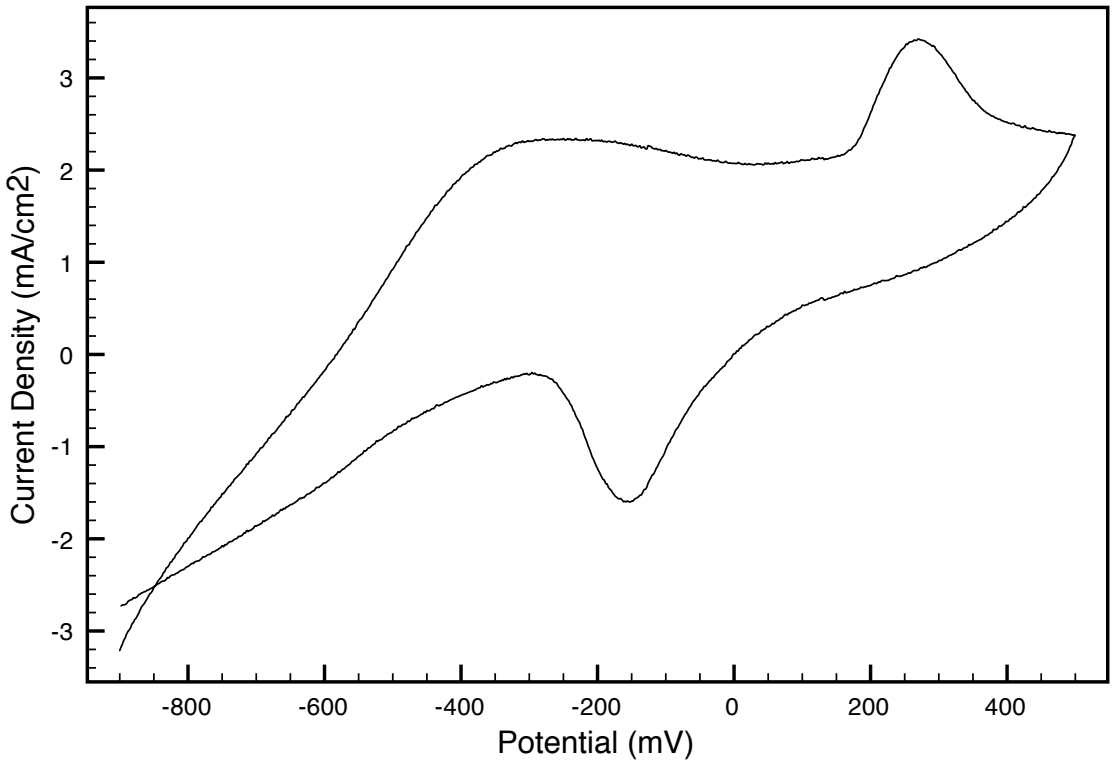

Figure 3.13: Cyclic voltammogram of Ag deposited into a metal-backed AAO template. Potential referred to reference electrode.

the deposition of CdSe, the potential was alternated between -350 and -800 mV based on analysis of the cathodic scan of the cycle in the cyclic voltammogram collected for this electrolyte, which is well correlated with potential deposition ranges suggested in literature by Kressin.(Kressin et al., 1991) A binary semiconductor of near stoichiometric proportions is desired and can be produced by depositing CdSe in equal proportions. At a potential of -350 mV, CdSe and Se is deposited at rates equal to or less than the diffusion limited rate in submonolayer quantities (for CdSe) and far less for Se based on the rate of deposition which is determined by the concentration of the species in solution and the rate of current passing through the cell. At lower potentials (-800

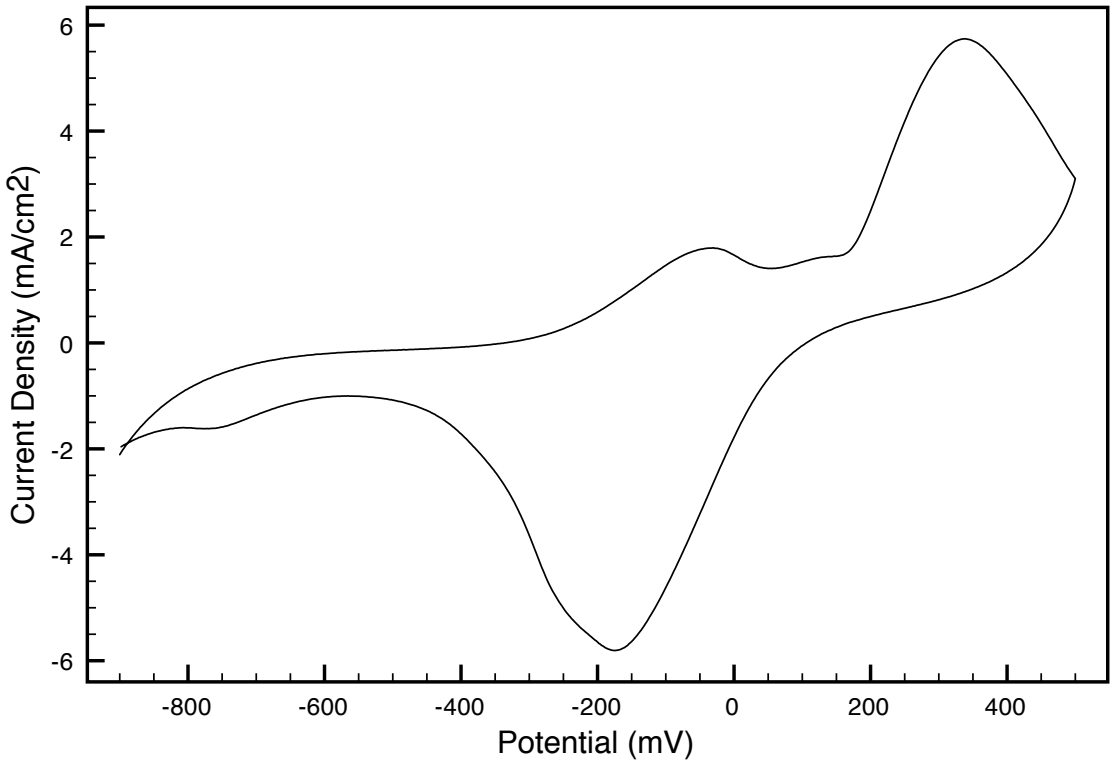

Figure 3.14: Cyclic voltammogram of Au deposited into a metal-backed AAO template. Potential referred to reference electrode.

mV) bulk Cd is deposited in excess during the remainder of the cathodic scan. The Cd that has not reacted with selenium is then stripped off, which corresponds to the oxidative peak present in the anodic portion of the scan located at roughly -350 mV in the CV. Given the deposited CdSe is thermodynamically stable enough, it remains on the surface and the next cycle is initiated, resulting in the gradual deposition of CdSe, which proceeds at 7 $\mathring{A}$/s.(Kressin et al., 1991)

It's important to keep in mind that the reduction of Au and Ag from solution at -1 V is also accompanied by hydrogen evolution, which is evident in the pourbaix diagram in Figure 3.12. Thus, all of the energy introduced into the plating solution bath isn't

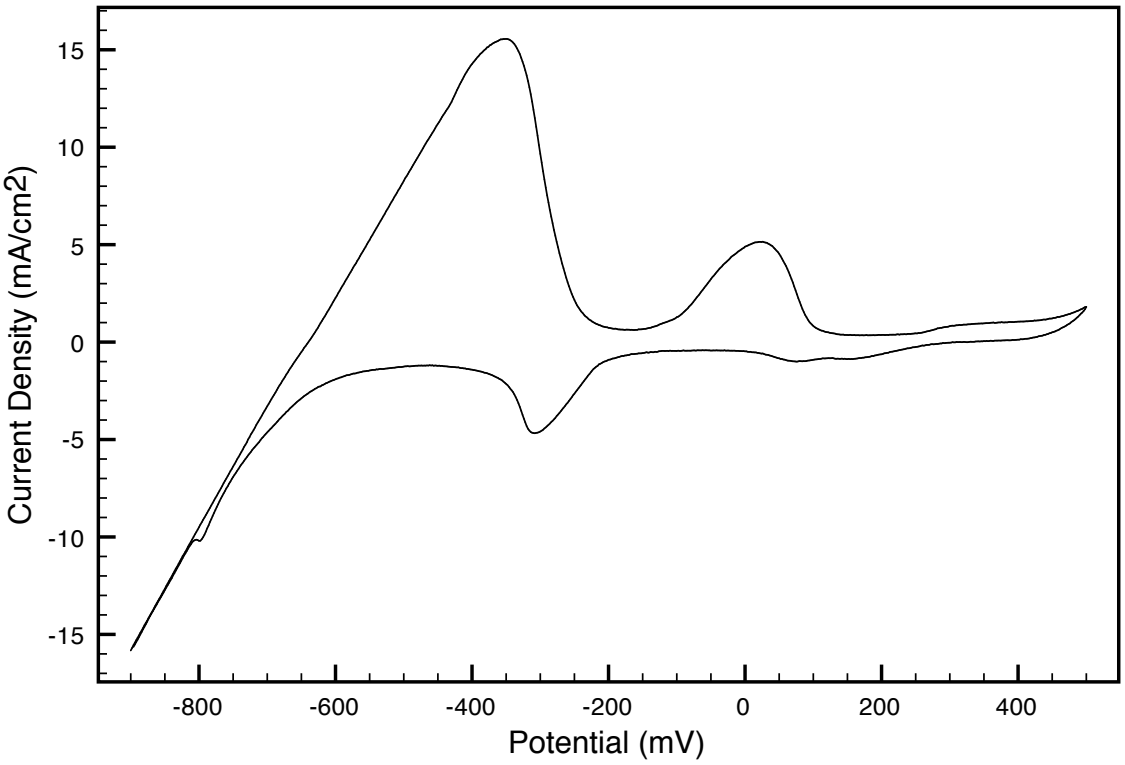

Figure 3.15: Cyclic voltammogram of CdSe deposited into a metal-backed AAO template. Potential referred to reference electrode.

used for the reduction of the ions present in solution and needs to be accounted for when monitoring the coulombs of charge passed through the cell when depositing nanowires, as the apparent length will routinely fall short of any theoretical values determined that do not take hydrogen evolution into consideration. The single material nanowires used here are generally composed of Au, and as such these will be the nanowires focused on in this work.

3.3.2 Materials and Instrumentation

A commercial potentiostat (PST050, Radiometer Analytical) is used to electrochemically deposit the nanowires into the template with a Pt counter electrode and a Ag/AgCl (sat KCl) reference electrode. Ag plating solution (Silver 1025, Technic Inc.) and Au plating solution (Orotemp 24, Technic Inc.) were obtained from the respective manufacturers. NaOH, ethanol (Fisher Scientific) and HNO_3 were all obtained from Fisher Scientific. Contact angle measurements were obtained using a CCD camera and a home-made XYZ positioning stage. High purity aluminum (Alfa Aesar, 99.998% pure, 0.5 mm thick) was also obtained from Fisher Scientific.

3.3.3 Experimental

3.3.3.1 Preparation of AAO templates for electrochemical deposition of metallic ions from solution

The preparation of the AAO templates used for the electrochemical deposition of metals inside the pores begins with the thermal evaporation of Ag onto one side of the template. A special metal sheet with nine holes slightly larger than the dimensions of the AAO templates themselves (13 mm in diameter) except for a small segment at the bottom with dimensions of 12 mm in diameter is used as a holder for the templates in the thermal evaporation chamber and was fabricated in house by the machine shop. The holder is suspended from a standard sample stage at an angle using clips and thin metal wires. We found that keeping the stage tilted while evaporating the metal

covers the holes and allowed us to skip the step performed by others(Yu et al., 2000) of electrochemically depositing more Ag onto the backside of the template before the actual nanowires are deposited.

The AAO templates are placed shiny side down into the template holder before it is suspended from the sample stage. This side of the AAO template is often referred to as the branched side as the pores here do not typically run parallel to each other and are interconnected, which is likely a by-product of the deposition method used to separate the alumina templates from their underlying aluminum substrates.(Routkevitch et al., 1996)(Jessensky et al., 1998)(Tian et al., 2005) This orientation is chosen to facilitate the electrochemical deposition of Ag, which allows the rest of the template to be filled with the metal of choice while generally not having to be concerned with more branching at a later segment of the channel.

Metal is typically evaporated onto the substrates at a rate between 5 and 50 nm/s. Performing the evaporation at a lower rate did not appear to have any noticeable benefits, as this layer is only meant to serve as a conducting layer permitting the template to be an electrically active component in the series of components that comprise the circuit that defines the cell while being consistent (i.e. non-porous) enough to provide a good base substrate for the electrochemical deposition of additional metal into the pores of the template itself. The prepared templates are stored in a container at atmospheric conditions until further used.

The prepared AAO templates are placed into the electrochemical cell with the thermally evaporated metal later facing the working electrode. The cell is assembled,

and then filled with Ag plating solution. The Ag layer deposited here is used as a sacrificial layer as the bottoms of the AAO pores are not parallel and exhibit significant branching. Deposition was performed by using the chrono coulometry method of the Voltalab software. The deposition was performed at -1 V and was allowed to proceed until -2 C of charge was passed through the cell based on the integration of current versus time (automatically performed by the software). This step is typically completed within 10 minutes, and the cell is rinsed with distilled water 3x before proceeding to the next step.

3.3.3.2 Formation of single material nanowires

Deposition of Au proceeds immediately after the deposition of the sacrificial Ag layer. The deposition of this metal generally employed the chrono coulometry method since the lengths of the nanowires could be controlled by specifying the amount of charge that should be allowed to pass through the cell before the method is terminated. This length is also dependent on the surface area available on the working electrode for deposition which is defined by the cell itself. For lengths of nanowires longer than 500 nm, the potential was set to -1 V and a quantity for the limiting charge was set accordingly, although -1.2 V for the potential was also used here on occasion without any observable consequence. For nanowires shorter than 500 nm, the potential was typically set to -0.55 V, as this was found to allow the reduction of the metal to proceed more slowly which permits metal to be deposited more uniformly over the entire cell and is important when thin layers (as little as several tens of nanometers in

some experiments) are being constructed.

This step is completed with the rinsing of the cell three times with distilled water after deposition is complete.

3.3.4 Formation of heterostructure nanowires

Heterostructure nanowires were formed by immediately depositing a secondary (semi-)metal after the deposition of a primary metal, followed by the deposition of the primary metal again to create a 'sandwiched' secondary metal trapped between two layers of the primary metal. The secondary material used here was generally the semiconductor CdSe, although other metals such as Co and Fe were also deposited successfully using the same technique.

Based on the discussion outlined in section 3.3.1, the semiconductor CdSe was deposited by using the chrono amperometry method. Potential 1 was set to -0.35 V, while potential 2 was set to -0.80 V, which constitutes one full cycle of deposition. By making use of the observation that 1 cycle corresponds to 7 $\mathring{A}$, the number of cycles can be set in the software depending on the desired length of the nanowire segment. The voltage cycling rate was approximately 11.1 Hz, which corresponds to the rate used previously by others.(Klein et al., 1993)

3.3.4.1 Formation of arbitrarily functionalized nanowires in AAO templates

A schematic of the process described in this section is presented in Figure 3.16 for clarity. Typically, metals are deposited directly into AAO templates after one side has been coated with a metal, producing nanowires with unmodified surfaces. It is possible to deviate from this and construct nanowires with arbitrarily functionalized surfaces by first absorbing a self-assembled monolayer (SAM) onto the surfaces of the template followed by the subsequent reduction of the material of interest into the pore channels. Several methods can be used to coat the AAO templates with SAMs, including liquid phase and vapor phase techniques.

The vapor phase deposition was primarily used here to coat the AAO with a molecular monolayer of (3-mercaptopropyl)trimethoxysilane (MPTMS), both on the remaining face of the AAO (not coated with thermally evaporated Ag) and inside the pores using a modified method initially devised by Ledung et al.(Ledung et al., 2001) Specifically, two AAO templates with metal evaporated onto one side of the template are placed on one side of a medium sized polystyrene (PS) dish, metal side down. The top and bottom halves of a smaller PS dish are placed inside the larger dish away from the AAO templates. Next, 200 μL of distilled water is placed into one half of a dish, and 100 μL of MPTMS is placed into the other. The larger PS dish is then sealed and placed into an 80 C oven for 90 minutes, which permits the immobilization of MPTMS onto the surfaces and into the pores of the AAO.

The MPTMS-functionalized template is placed into the electrochemical and is pre-

pared with thermally evaporated Ag as described in section 3.3.3.1. Next, an Au nanowire segment is deposited as is outlined in section 3.3.3.2. Subsequently, by placing the partially filled template briefly into the chamber of an oxygen plasma cleaner set to 100 W, the immobilized molecular monolayers can be removed from the surfaces of the template where metal has not already been deposited, which cleans the surface of any carbonaceous material and leaves a fresh metal oxide surface in its place, which can be later used for the attachment of another molecular monolayer that follows any of several standard attachment routes via silane chemistry.

After the plasma cleaning step is complete, the AAO template is removed from the chamber and placed into distilled water in an ultrasonicator for 30 seconds to aid in the removal of any nonspecifically bound residue material from the outer surfaces and inner pores of the template. The AAO template is rinsed again in methanol, and is then placed back into the electrochemical cell for the plating of the next material.

At this point, one of two routes is possible; either CdSe is deposited(Kressin et al., 1991) for the formation of functionalized heterostructured nanowires, as outlined in section 3.3.4 or more Au can be deposited for functionalized single-material Au nanowires as is outlined in section 3.3.3.2. For heterostructured nanowires, the cell is rinsed 3x with distilled water, and the AAO is removed in order to attach another layer of MPTMS before more Au is deposited into the AAO for the third and final segment of the nanowire. After the final Au segment has been deposited, the SAM removal step is repeated and the AAO is rinsed.

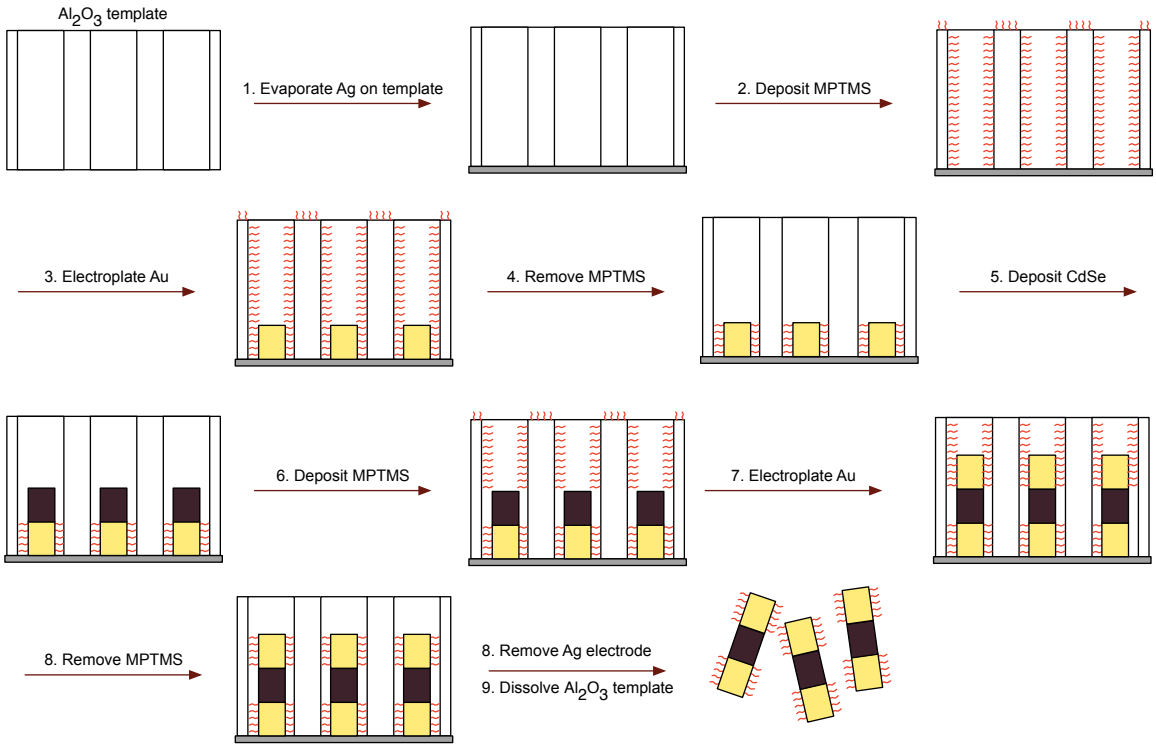

Figure 3.16: Preparation of selectively functionalized heterostructured nanowires. (1) Ag is evaporated onto the AAO template. (2) The template is coated with MPTMS through a vapor-phase reaction. (3) Au is electrodeposited into the AAO. (4) The template is placed into a plasma cleaner to remove MPTMS not bound to the surfaces of Au nanowire segments. (5) CdSe is electrodeposited into the AAO on top of the already-deposited Au segments. (6) MPTMS is deposited again through a vapor-phase reaction. (7) Au is electrodeposited into the AAO. (8) MPTMS is removed. (9) The evaporated Ag is removed with nitric acid. (10) The AAO template is dissolved with 0.05 M NaOH.

3.3.4.2 Release of nanowires

Upon completion of the nanowire deposition the Ag deposited in and on the AAO is removed by submerging the AAO into a diluted solution of nitric acid in order to remove the thermally evaporated and electrochemically deposited Ag layers, and is then rinsed with distilled water. The nanowires are released from their template by immersing the AAO in a 0.05M solution of NaOH and are left overnight until the AAO is completely

dissolved, producing free nanowires. Particulate matter resulting from dissolution of the AAO is removed by washing the nanowires 3x in ethanol via centrifugation for 20 seconds or more at 8000 rpm.

3.3.5 Results and discussion

3.3.5.1 Nanowire morphology

The electrochemically deposited nanowires described in this section differ drastically from the nanowires fabricated via the electroless deposition route described in section 3.2. Figure 3.17 shows a typical example of the Au nanowires that are formed after the successful reduction of the metallic ion from solution. Several differences between these nanowires and the electroless Au nanowires are immediately apparent. The first difference is observed in the morphology of the surface of the nanowires. The nanowires depicted here have surfaces with very little roughness, unlike the nanowires shown in figure 3.8. This can most likely be attributed to differences in the deposition mechanism of metallic ions from solution. The electric field present in the electrochemically deposited nanowires makes the working electrode (i.e. the upper-most surface of the nanowire exposed to the solution inside of the pores of the AAO template) the most energetically favorable position for metallic ions to exist in while in solution. Once the ions are in close enough proximity to the working electrode, electrons are transferred uniformly from the exposed surface to the ions in proximity, making these ions become part of the working electrode and causing the nanowire to slowly increase in length, being constrained in morphology only by the AAO template itself.

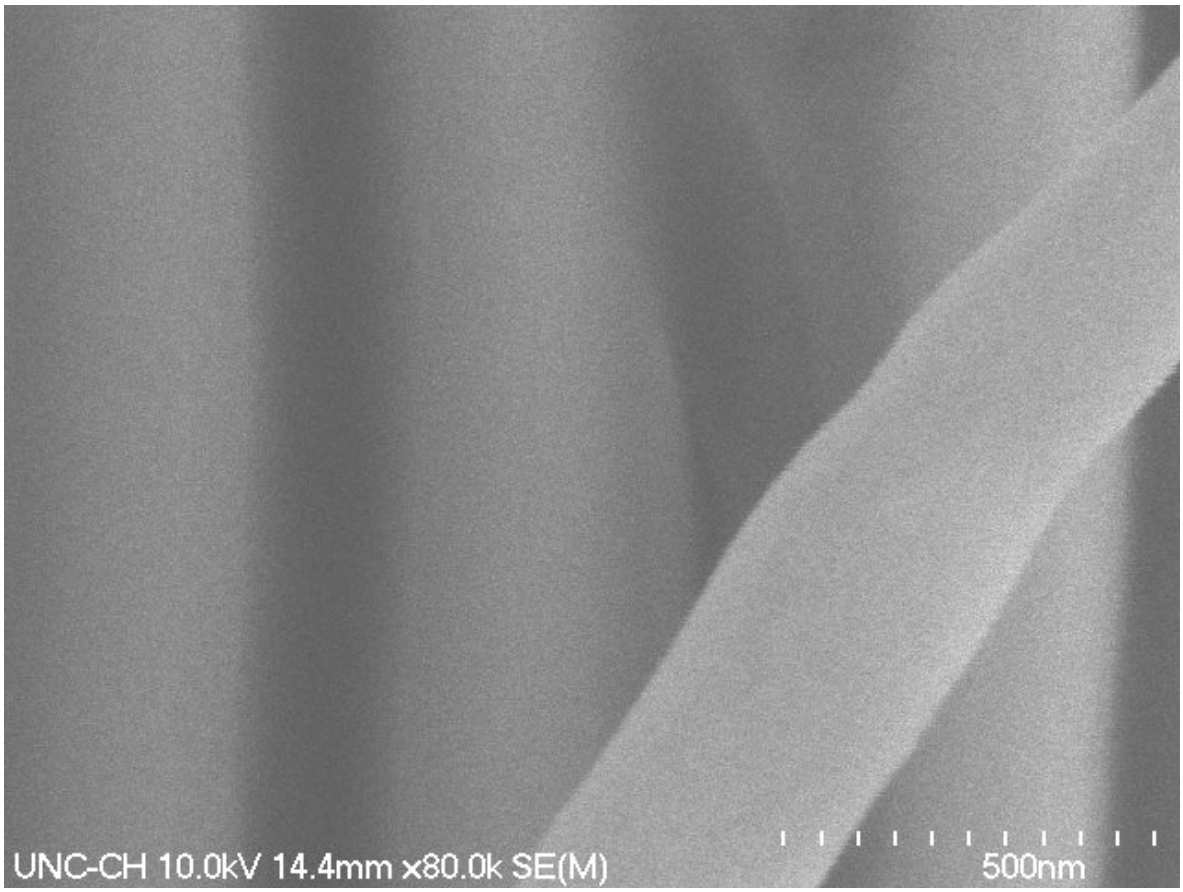

Figure 3.17: High magnification scanning electron micrograph of Au nanowires formed via the electrochemical deposition of Au into AAO templates. The pores are rated as 200 nm in diameter, although the nanowire is substantially larger and close to 350 nm.

The nanowires produced in figure 3.8 via the electroless route have no electric field present as is true for the electrochemically deposited nanowires, and these nanowires presumably form based on a competition between gold ions forming small clusters in solution in order to reduce their total free energy, and adhesion to a surface once the clusters in solution reach a critical diameter. The existence of these clusters in solution is less favorable energetically than the surfaces of PCTE, and this competition between cluster formation and adhering to an activated surface is likely the source of

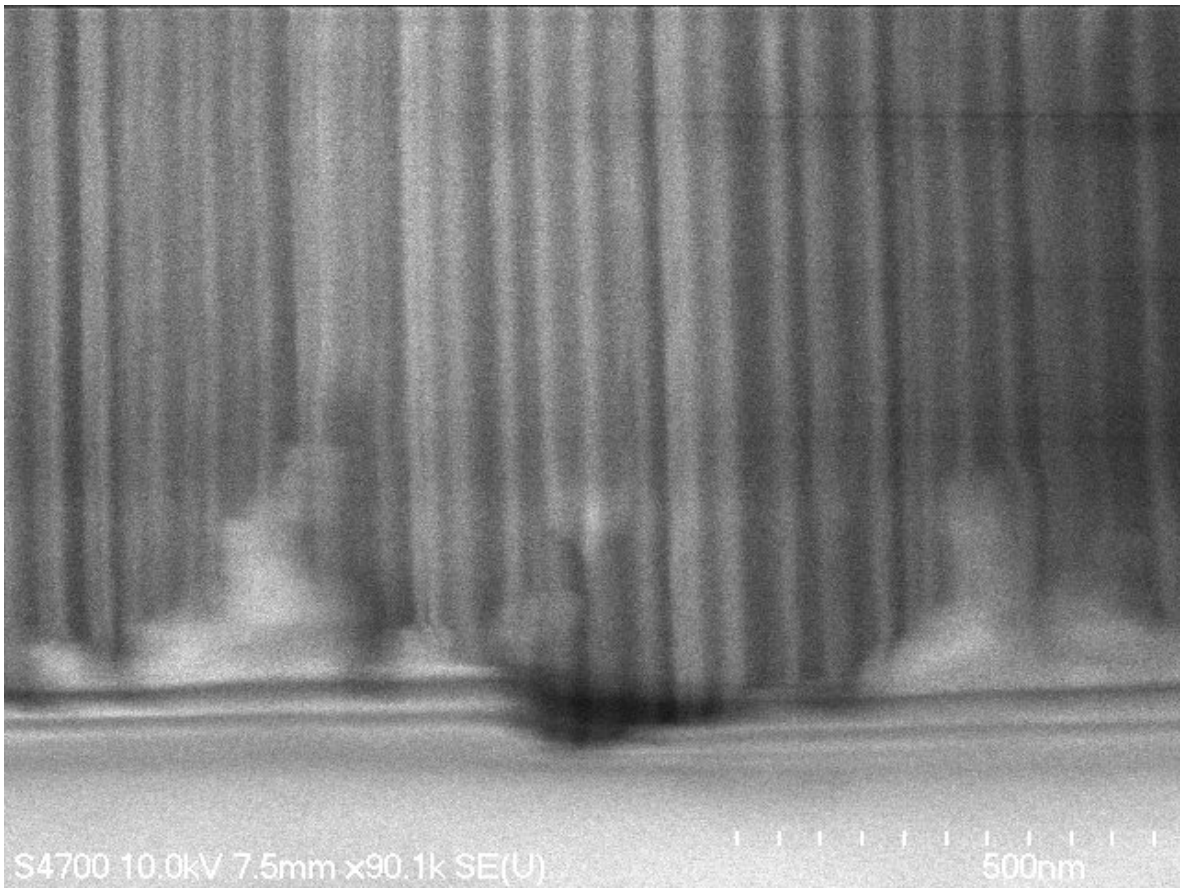

Figure 3.18: Tilt-stage capture of a homemade AAO broken in two and fabricated by anodization in 0.3M oxalic acid at 40 V.

the clumpy nature of these nanowires. One possible method of reducing this roughness is to reduce the amount of Au initially present in solution before the reaction begins by the activation of the solution with formaldehyde. This reduces the size an individual Au cluster can grow by reducing the amount of Au present in solution to become part of a cluster, which in turn increases the chance that the cluster will come into contact with the energetically favorable surface of the PCTE before its cluster size can increase to a size where it begins to largely contribute to the roughness of the nanowire itself. As previously noted, both PCTE and AAO templates are known to have smooth surfaces

which rules out any contribution from the template itself causing being the source of the nanowires formed by the electroless reduction technique.

On the other hand,figure 3.17 also shows that although the surfaces of the electrochemically deposited nanowires do appear to be smooth, the diameters of the nanowires are not consistent. To the best of our knowledge, this appears to be one of several artifacts of the AAO templates as provided by the manufacturer. SEM images of AAO templates fabricated in-house do not appear to have this same deficiency as the diameter of the inner pores appear to be consistent, as is visible in figure 3.18.

3.3.5.2 Nanowire functionalization

Until now, previous nanowire functionalization schemes have exploited differences in the composition of the nanowires themselves in order to attach different molecular monolayers.(Nicewarner-Pena et al., 2001; Salem et al., 2003) This technique in not applicable to nanowires composed of single materials or to nanowires composed of a multiple materials but with similar chemical affinities for the same functional group. This limitation applies to the heterostructured nanowires described here, as both Cd and Au compounds both have similar affinities for mercapto groups, and they are readily absorbed onto Au and CdSe surfaces.(Pena et al., 2002; Aldana et al., 2001; Niemeyer et al., 2003) This limitation is circumvented by forming a protective surface on selected regions on the surface of the nanowire as they are deposited into the template. This protective layer is constructed through the addition and removal of a bifunctional molecular monolayer that is first attached to the template and then to the

nanowires themselves as they are formed within the pores of the template through the electrochemical reduction of metallic ions in solution. The addition and removal of the SAMs permits the definition of regions of the nanowires that are either available in a subsequent step for the adsorption of other molecular monolayers or masked off during later processing steps. These other molecules may include but are not limited to other SAMs and DNA.

The bifunctional modifier MPTMS was selected as the monolayer for nanowire functionalization since it is capable of forming covalent bonds with other silanes and metal oxide surfaces(Wang et al., 2003) and because of the high affinity between noble metals and thiolate groups.(Grabar et al., 1995) It was postulated that the silane of MPTMS would react with the surface of the AAO template during the vapor phase deposition step as the AAO template is a ceramic composed of aluminum oxide (Al_2O_3) which would leave the pores of the template coated with a reactive thiol group as this has been previously observed with similar compounds.(Wang et al., 2003)

Before experiments were initiated on selectively functionalizing the surfaces of the AAO templates and subsequently the surfaces of the nanowires themselves, experiments were first performed on bare aluminum substrates, making use of the native oxide inherent on any bare aluminum surface that has been exposed to ambient conditions(Li et al., 1998) as a model surface that mimics the composition of surfaces of the AAO template. These flat aluminum surfaces were deemed to be more applicable for the collection of contact angle measurements than the porous AAO templates since the porous nature of the template surface may cause inconsistencies with measurements of

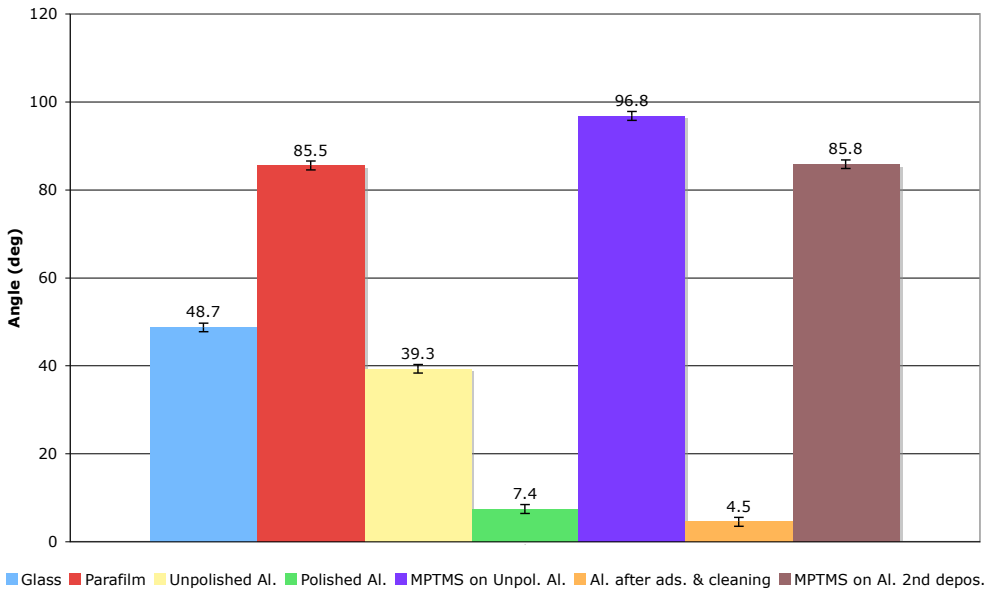

Figure 3.19: Contact angle measurements of water drops on various substrates.

water drops on the surface.

All surfaces were cleaned with acetone, distilled water and methanol and dried under a nitrogen stream before use. 10μL water drops were placed onto substrates using a micropippetor and were measured with a goiniometer to determine contact angles.

Cleaned aluminum and glass substrates were first used as controls and compared to contact angles found in literature.(Sklodowska et al., 1999) Once the contact angles collected from these samples were found to be well correlated with previous values (difference $\leq 5\%$), similar experiments on modified metal oxide surfaces were performed.

The surfaces of the aluminum substrates were modified by forming SAMs of MPTMS through a vapor phase deposition process (see section 3.3.4.1 for details). Contact angles of the substrates were collected after the initial surface modification and were found to be larger than the unmodified surfaces by almost a factor of 2. This is possibly due to hydrophobic interactions between the water drop and the –SH terminus of the bifunctional modifier as the siloxyl group is bound to the metal oxide surface of the substrate.(Chrisey et al., 1996) These data suggested the surfaces of the examined substrates have indeed been modified, based on the change of the contact angle of water drops placed on these surfaces, and that this method may prove to be useful if the modified surfaces can remain intact during the electrodeposition of metal into AAO templates modified in a similar manner.

More interestingly, however, is the reversibility of this process. Ideally, if SAMs can be attached to substrates repeatedly, this could open up a door that allows arbitrary regions of a substrate to be chemically altered or left unmodified during sequential electrochemical deposition steps. Two things need to be observed for this to occur: the monolayers need to be easily removable and subsequent monolayers need to be re-attachable to the same substrate. Modified substrates were cleaned of the attached SAMs by placing the substrates in the chamber of an oxygen plasma cleaner for 5 minutes in order to remove carbonaceous material (ie. the SAMs) from the substrate. Contact angles of water drops were collected again on these substrates and found to be drastically less than the original unmodified aluminum substrate and even comparable to substrates that had been electrochemically polished. This indicates that the SAMs

are easily removed by an oxygen plasma. Additionally, SAMs that were reattached to these substrates also showed contact angles with values close to the original contact angle values but were slightly less than what was originally observed. This may be a result of the reduction of the surface roughness of the oxide layer on the aluminum substrates, as similar behavior has been observed previously in silicon substrates with an oxide layer that have been exposed to an oxygen plasma.(En and Fisher, 2004)

Due to the potential applicability of this technique for the formation of arbitrarily surface-modified nanowires, experiments were then conducted on AAO templates using this method. Figure 3.20 displays both bright-field and fluorescence images of the functionalized nanowires obtained by this technique. Parts A and B of Figure 3.20 show nanowires constructed by depositing the semiconductor CdSe between two Au layers. MPTMS is attached to the pores of the template before depositing the segments of Au. This layer is then removed from the surfaces of the pores where Au has not yet been deposited by oxygen plasma cleaning the template. After release of the nanowires, samples were obtained that have been functionalized with MPTMS only along the Au segments of the nanowires and not the intermediate CdSe segment. In order to demonstrate the selectivity of this process, thiolated single-stranded DNA (5'-GGGCGGCGACCT-3'-C6-disulphide oligonucleotide, UNC Pathology) was bound to the still exposed surfaces based on a previously published procedure.(Kovtyukhova et al., 2001) The oligos absorb only to the unmasked regions of the nanowire as these regions are the only portions that have not yet had their surfaces coated with any other SAM. The DNA was then labeled fluorescently with a DNA-binding fluorescent

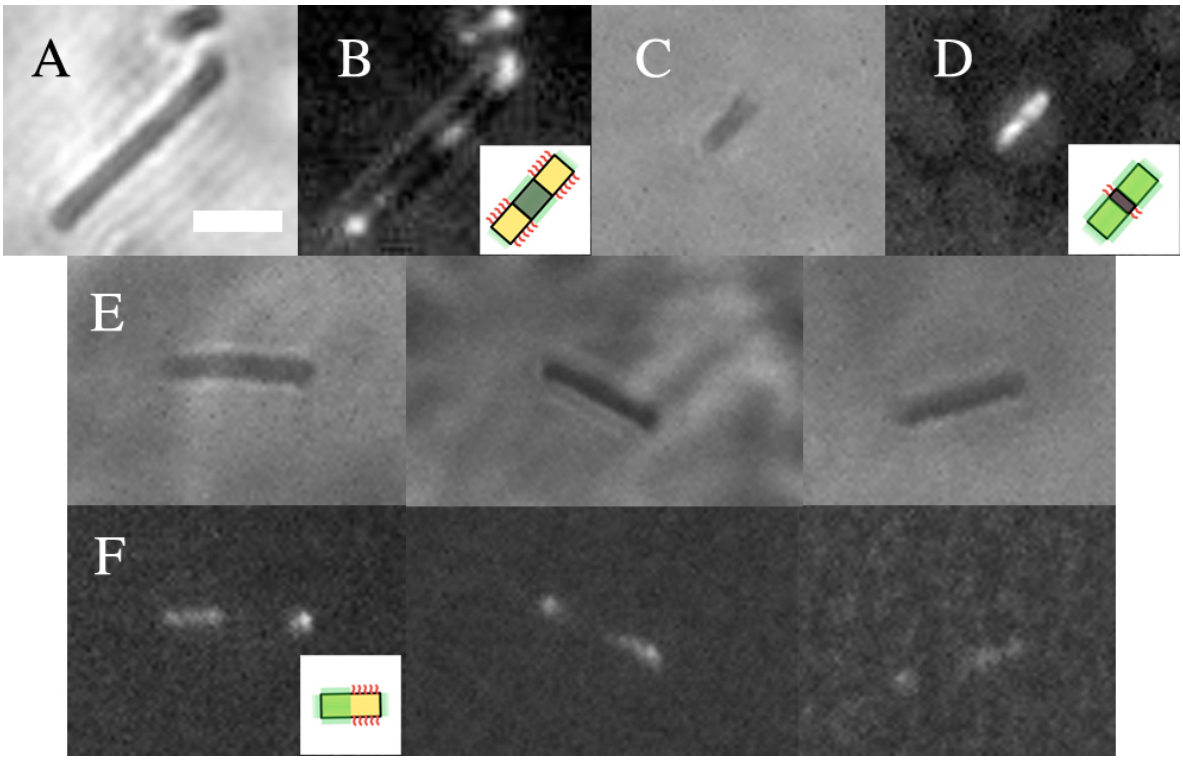

Figure 3.20: Optical and bright-field micrographs of nanowires protected at specific sites, functionalized with thiolated DNA and subsequently labeled with a fluorescent dye. Insets contain schematics of the designed fluorescence, where areas in green correspond to fluorescently labeled DNA bound to the nanowires and red lines denote the locations of the protective monolayer. (A) Bright-field micrograph of Au-CdSe-Au nanowires with Au protected sites. (B) Fluorescence micrograph denoting sites that have been functionalized with thiolated DNA. (C) A shorter Au-CdSe-Au nanowire with a protected CdSe region. (D) The resulting fluorescence micrograph. (E) Au nanowires, each with half of its length protected with MPTMS. (F) Fluorescence micrographs of the same nanowires showing where DNA has absorbed to the surface. An oil immersion 100x objective was used for each micrograph. The scale bar in (A) is 3 μm.

dye, YOYO-1 (Molecular Probes). As is evident from the fluorescence images, the dye binds preferentially to the regions of the nanowires that had been unmasked after the functionalization process, leaving the masked portions dark and indicating the success of the functionalization process.

It is also worth noting that DNA binds to the extremities of the nanowires. This

is a result of the nanowires' ends being exposed either to the Ag backing that forms the initially electrically active component of the working electrode or directly to the plating solution. In either case, the masking SAMs are unable to bind directly to the extremities of the nanowires as the thiolate groups are either already absorbed to the Ag or are not present until after the nanowires themselves have already been deposited into the pores of the template. This artifact can be circumvented if the material deposited at either end of the nanowire can be selectively removed after the nanowires are released from the template.)

Parts C and D of Figure 3.20 contain bright-field and fluorescence images of nanowires deposited in the presence of MPTMS complementary to the conditions described above. Accordingly, these nanowires exhibit a small gap in the image fluorescence emission which is visible in Figure 3.20D and corresponds to the 700 nm long MPTMS-protected CdSe segment of the nanowire, deposited from 1000 individual cycles of CdSe electrodeposition(Kressin et al., 1991) based on the conditions of our experimental setup. The length of this CdSe region can easily be reduced to the nanoscale (dimensions of 20 nm and less have been constructed and examined by SEM microscopy), but the optical detection of segments this miniscule will require more elaborate methods than what was employed here.

The robustness of this technique is demonstrated through the application of the functionalization method on nanowires composed solely of Au. Corresponding bright-field and fluorescence images of single material nanowires are shown in Figure 3.20E. Nanowires of this form were fabricated in the same manner that the heterostructured

nanowires above were fabricated, except the Au plating solution was not exchanged for the semiconductor solution between deposition steps. The same artifact discussed above is also evident in Figure 3.20F.

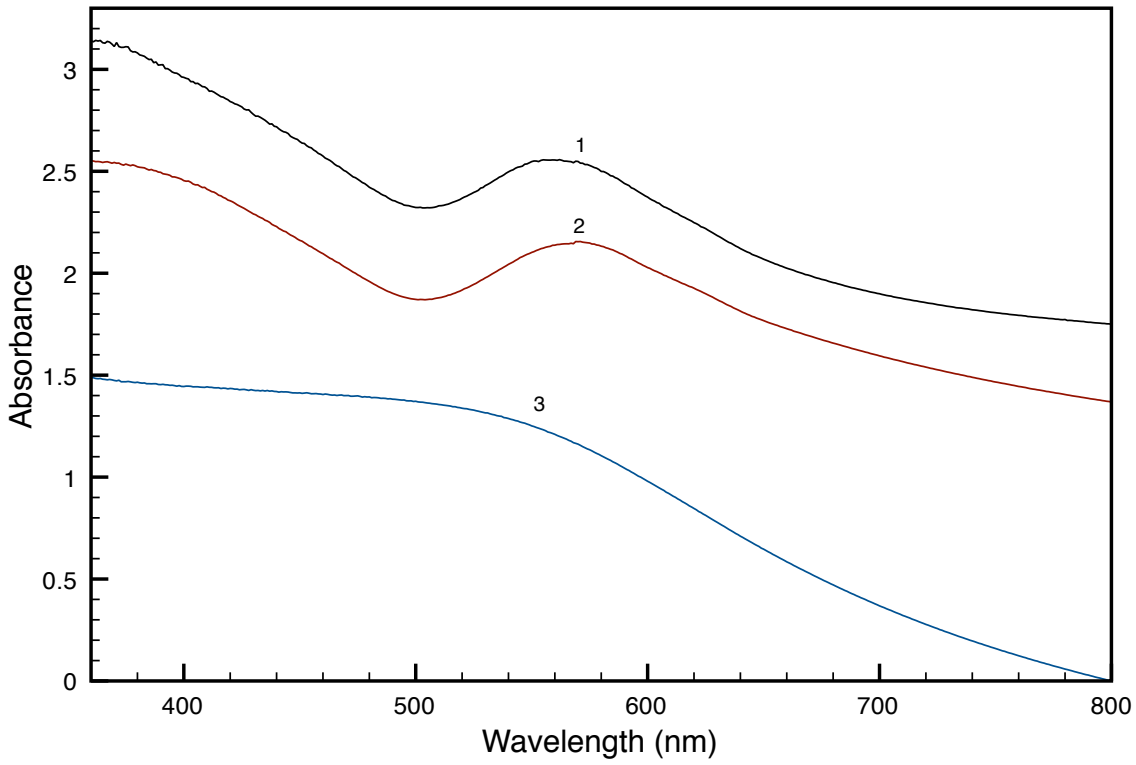

Figure 3.21: UV–visible spectra for Au nanowire/AAO composites and a blank AAO template. Curve 1, 200 nm Au nanowire/AAO composite functionalized with MPTMS; curve 2, 200 nm Au nanowire/AAO composite; curve 3, blank AAO template.

The vapor deposited SAMs of MPTMS are believed to form an effective chemical resist on the surfaces of the pores within the AAO template. Thus, SAMs that have not specifically bound to the surfaces of the nanowires are easily removed and leave the surface of the AAO template in a pristine state which permits the subsequent attachment of other molecular monolayers. Methods other than plasma cleaning should

be applicable here as well for the removal of these non-specifically attached monolayers, including employing the use of a piranha solution (4:1 M_2SO_4 / 30% H_2O_2) which may also be effective here. [Warning: piranha solutions react violently with organic material and should be used with extreme caution!]

Based on previous experiments(Mulvaney, 1996; Bellino et al., 2004) it is now well known that the surface plasmon absorption band of metal nanoparticles is sensitive not only to the size of the nanoparticles but also to the degree of aggregation between particles and to the presence of complexed surface molecules. Figure 3.21 contains UV–visible absorption spectra of Au nanowires roughly 1 μm in length that have SAMs of MPTMS on the surface of the nanowires. The nanowires here are still retained in the AAO templates in order to reduce the observable broadening of the absorption peak maximum that occurs when nanowires with larger diameters are oriented randomly. Curve 3 contains the spectrum of a plain AAO template with 200 nm pores. Curve 2 is the spectrum of an AAO template that has 1 μm long nanowires deposited into the pores with a maximum absorption value near 560 nm. Curve 1 is the spectrum of Au nanowires of the same length but that have been coated with MPTMS along the entire length of the nanowire. In this experiment, both the diameters of the pores and the amount of Au deposited into the AAO template remain constant between the two templates, thus the relative difference in intensity of the absorption peaks as well as the slight shift in the position of the peaks between curves 1 and 2 can be attributed to to the presence of MPTMS on the surface of the nanowires. This difference may correspond to a measurable difference in the local refractive index due to depletion

near the surfaces of the nanowires. Further work may be needed to clarify the details of these observed differences and the relationship to the amount of material absorbed to the nanowires.

Chapter 4

Electrical Characteristics

4.1 Introduction

Quasi-one-dimensional semiconductor materials such as nanotubes and nanowires have been studied in recent years due to their potential for use in applications requiring active electrical components for computer circuitry. These structures can often be isolated and individually addressed, and are also good candidates for the interrogation of device behavior at this scale, which typically varies significantly from its bulk counterparts. Materials studied to date include but are not limited to CNTs(Hazani et al., 2004), ZnO(Zheng et al., 2002), Si(Hisamoto et al., 2000), BiTe(Sander et al., 2002), CdSCo(Yoon and Suh, 2002) as well as some organic materials(Chung et al., 2005; Park et al., 2004a). New materials are constantly being discovered, and cadmium selenide (CdSe) is one material that has received considerable attention as it is a direct bandgap material that possesses good optoelectronic properties and shows excellent stability in wet photovoltaic cells.(Murali et al., 2004) Nanostructures have been constructed that include test beds for the exploration of quantum confinement

theories(Peng et al., 2000), multicolor lumiphores(Torimoto et al., 2006), multishell nanocrystals(Xie et al., 2005), and quantum dots that exhibit stability over a wide range of pH values and ionic strengths(Palaniappan et al., 2006). Fabrication methods used to produce structures include aqueous and organic solution routes(Chaure et al., 2005), MBE(Eich et al., 2000), and template methods making use of photochemical synthesis(Zhao et al., 2004b) and electrochemical deposition.(Pena et al., 2002; Kovtyukhova et al., 2004)

Klein was one of the first to produce arrays of cadmium chalcogenide nanowire arrays in porous alumina (PA) templates and examined the $I - V$ response by performing sweeps on the entire array embedded within the template.(Klein et al., 1993) Pena(Pena et al., 2002) and Kovtyukhova(Kovtyukhova et al., 2004) have also constructed nanowires in PA templates, using the regular size and spacing of the individual pores of the structure to create nanowires with well defined diameters and lengths. Their investigations on electrical transport through CdS nanowires addressed the effects of photoelectric induced currents. Coaxial structures made from CdSe nanowires surrounded by a SiO_2 gate dielectric were also explored. Their investigations on these structures were primarily focused on CdS nanowires, and information including the carrier mobilities were obtained, but for CdSe nanowires properties such as carrier mobilities, carrier densities and resistivities were not explored.

This chapter extends the findings of Kovtyukhova et al. and provides information about these structures beyond the carrier mobilities alone by examining the electrical transport characteristics of heterostructured metal-semiconductor-metal nanowires

fabricated by the electrochemical reduction of metal and semiconductor ions from solution into PA templates - specifically, in the past, widely varying numbers have been reported for various properties of nanostructures composed of the same material due to the methods used to extract these parameters. For this reason, a quantitative method is used to analyze the electrical properties of these structures and to determine how they may be improved. The nanowires fabricated within PA templates are first released and then suspended in solution before being deposited onto optically patterned substrates and then linked electrically to large metal pads through electron beam lithography. A Si/SiO_2 substrate is then used as a backgate to modulate the conductance of individually addressed nanowires.

4.2 Background

The method typically used when analyzing the carrier mobility of a nanowire is the field-effect-transistor (FET) model which assumes there is an ideal insulating layer separating the conducting channel of cylindrically-shaped structures from the gate but is otherwise identical to routinely used planar models.(Zhang et al., 2007b) In most cases, the assumption about the shape of the insulating layer is inaccurate since this insulating layer doesn't surround the entire channel of the device. The model employed here accounts for both the nature of the contacts formed between the metal and semiconducting portions of the nanowire as well as the contribution from channel of the nanowire itself. By using structures that have channels on the order of a micron long,

the transport mechanism of the majority carriers lies in the diffusive regime and isn't dominated by ballistic transport (as is true for nanowires only several tens of nanometers long) and an Ohmic law in addition to the effective mass approach can be used to describe the transport behavior of the majority carriers in the undepleted portion of the nanowire.(Zhang et al., 2007b) The nature of the contacts also play a very important part in determining the structure of I-V curves obtained from experimental devices, and a thermionic field emission model can be used to adequately describe the metal-semiconductor interface. Zhang et al. showed that all variations in shape of experimentally obtained I-V curves can be obtained using this quantitative analysis model, and parameters including the carrier mobility and resistivity of the nanowires can successfully be extracted.

In order to collect data about the intrinsic properties of semiconductor nanowires produced via electrochemical deposition, the semiconductor must be brought into contact with metal electrodes which are ultimately connected to a measurement tool that performs data collection. The two metal electrodes at each end of the semiconductor produce two Schottky barriers. Intimate contact between the semiconductor and the metal electrode is often desired, and to this end the metal electrodes are deposited *in situ* in order to minimize the presence of insulating contaminants between these these two components which will create an insulating barrier in series with the barrier formed between the metal electrode and the semiconductor of the nanowire. The height of these barriers collectively determine whether the I-V characteristics of the nanowire can be described as almost linear, almost symmetric, almost asymmetric or asymmetric. In

the case of the Au-CdSe-Au nanowires produced here, I-V the curves can be described as symmetric or almost asymmetric even though the same nanowires are produced and contacted with identical metal electrode and semiconductor 'channel' materials.

The asymmetrical nature of the I-V curves of these nanowires can be accounted for upon closer examination of Thermionic Field Emission (TFE) theory proposed by Padovani and Stratton.(Padovani and Stratton, 1966) TFE theory can be formulated as Thermionic Emission (TE) theory, but with an additional consideration of the reverse bias tunneling current that is ignored in TE theory. TE theory is most often applied in the modeling of plannar Schottky junctions. According to this theory, the current across a Schottky junction can be described by(Rhoderick and Williams, 1988)

$$J(V,\phi_b) = A^*T^2 exp\left(-\frac{\phi_b}{kT}\right) exp\left(\frac{qV}{nkT}\right) \times \left\{1 - exp\left(-\frac{qV}{kT}\right)\right\} \tag{4.1}$$

where A^*=$4\pi m^* qk^2/h^3$ is the Richardson constant of the semiconductor, ϕ_b is the Schottky barrier height, k is the Boltzmann constant, q is the magnitude of electronic charge, T is the temperature and n is a dimensionless quantity that describes the deviation of the Schottky barrier in the device from an ideal Schottky barrier where n=1, which can result from, for example, an interfacial insulating layer or image force lowering of the barrier height. This theory has been used often to analyze the forward I-V characteristics of nanowires, but it underestimates the reverse current as it predicts the current should saturate at very low values (tens of nanoamps). In a microelectronic system this is often the case and this amount of current is considered "leakage current"

under reverse bias conditions. However, in one dimensional nanoscale systems the reverse current is often on the order of tens to hundreds of nanoamps, and thus the device cannot considered to be "off" under reverse bias.

Under reverse bias conditions in TFE theory, tunneling through the reverse biased Schottky barrier is significant in a nanoscale metal-semiconductor-metal structure and such is the case for the nanowires fabricated here by electrochemical deposition. In particular, application of a moderate bias is enough for the potential barrier at the metal-semiconductor interface to become thin enough for tunneling of the majority carriers. The current through this barrier can be described by

$$J_1(V,\phi_b) = -J_{sy}(V,\phi_b) \times exp\left[V\left(\frac{q}{kT} - \frac{1}{E_0}\right)\right] \tag{4.2}$$

where J_{sy} is a function that varies slowly with applied bias given by

$$J_{sy} = \frac{A^*T(\pi q E_{00})^{1/2}}{k} \times exp\left(-\frac{\phi_b}{qE_0}\right) \times \left\{q(V-\zeta) + \frac{\phi_b}{cosh^2(qE_{00}/kT}\right\}^{1/2} \tag{4.3}$$

and ζ is the distance from the fermi level to the bottom of the conduction band, taken from bulk material values.(Rhoderick and Williams, 1988) The term E_0 is defined as

$$E_0 = E_{00}coth\left(\frac{qE_{00}}{kT}\right) \tag{4.4}$$

where

$$E_{00} = \frac{\hbar}{2}\left[\frac{N_d}{m_n^*\varepsilon_s\varepsilon_0}\right]^{1/2}. \tag{4.5}$$

E_{00} is a characteristic parameter in tunneling theory that describes the probability that an electron with energy equal to the bottom of the conduction band at the edge of the depletion region of the semiconductor is $1/e$.(Rhoderick and Williams, 1988) N_d is the density of donors at the interface of the metal-semiconductor junction, m_n^* is the effective mass of the electron in the semiconductor, ε_s is the permittivity of the semiconductor, and ε_0 is the permittivity of free space. The transition from TE to TFE is possible when

$$cosh^2(qE_{00}/kT)/sinh^3(qE_{00}/kT) < 2V_d/3E_{00} \tag{4.6}$$

taking into consideration V_d=$\phi_b/q - \zeta - V$. V has a positive value under forward bias and a negative value under reverse bias, so under reverse bias conditions, equation 4.6 is valid for larger values of V_d (i.e. when V has a negative sign and is under reverse bias conditions), and therefore the contribution of the tunneling current is more readily observable under reverse bias conditions. A metal-semiconductor-metal structure such as the Au-CdSe-Au nanostructure constructed here is typically modeled by TE theory. If the contacts are ohmic, the resulting $I - V$ curve will be linear. If one contact is ohmic and one is a Schottky contact the resulting $I - V$ curve will be rectifying. If both contacts are Schottky contacts with non-zero barrier heights formed between the metal-semiconductor interfaces, the resulting $I - V$ curve will be either symmetrical or almost-symmetrical depending on the size of the barrier heights at each junction. This difference in the barrier heights even for the same metal in contact at opposite ends of

the nanowire can result in an experimental $I - V$ curve that is asymmetric much like the ones often observed for the Au-CdSe-Au nanowires described here. Possible sources of this asymmetry are discussed below.

4.3 Experimental

CdSe FETs were fabricated electrochemically as a segment of stoichiometric CdSe sandwiched between two or more metallic segments. 200 nm Whatman, Inc. templates (manufactured by Anodisc) or 80 nm commercial PA templates fabricated by Synkera Technologies, Inc. were obtained and prepared for electrodeposition by thermally evaporating a thin metal layer of Ag onto one side of the substrate. A commercial PST050 potentiostat by Radiometer Analytical was used for the reduction of metal from solution into the PA template and was placed into a homemade cell and connected as the working electrode along with a platinum counter electrode and a Ag/AgCl (sat KCl) reference electrode. The cell was first filled with Ag 1025 plating solution by Technic Inc. and a sacrificial layer of metal was electroplated potentiostatically into the pores at -900 mV in order to fill the branched portion of the channels.(Kovtyukhova et al., 2001) The cell was then rinsed 3x with distilled water and filled with a commercial Oratemp 24 Au plating solution by Technic Inc., and metallic Au was deposited potentiostatically at -1000 mV, followed by an optional thin Ni segment (< 50 nm thick) was electroplated from a Watts bath (Nielsch et al., 2000) containing 300 g/L $NiSO_4 \cdot 6H_2O$, 45 g/L $NiCl_2 \cdot 6H_2O$, 45 g/L H_3BO_4 at pH 4.5. The CdSe segment of the nanowire was

deposited into the PA template based on previously published methods.(Pena et al., 2002) Subsequently, another optional Ni segment was electroplated after the electroplated CdSe segment of the nanowire was deposited, followed by another Au segment using the same parameters specified above to produce Au-Cdse-Au or Au-Ni-CdSe-Ni-Au heterostructured nanowires. After deposition the template was removed from the cell and rinsed with distilled water. Thermally evaporated and electroplated Ag was removed by carefully immersing the template into a solution of nitric acid (Fisher Scientific). The nanowires were then released from the template via immersion in a 3M NaOH solution for 15-30 min. The remaining undissolved particulate matter was separated from the nanowires by repeated rinsing with a combination of ethanol and distilled water (diH_2O) followed by centrifugation.

Devices were electrically contacted via electron beam lithography using pre-patterned substrates.(Williams et al., 2003) Macroscopic leads were fabricated on p^+Si/SiO_2 substrates with photolithography and nanowires suspended in ethanol/H_2O were subsequently deposited onto substrates from solution. The substrates were composed of a thermally deposited insulating oxide layer on top of a heavily doped p-type silicon wafer which is used as the gate material for the deposited nanowires. Electrical connections between the macroscopic electrodes patterned by photolithography and the deposited nanowires were formed by electron beam lithography on PMMA coated substrates and the evaporation of Ti/Au metal layers. All electrical measurements were taken in ambient conditions at room temperature using a Keithley 2400 Series SourceMeter and custom programmed National Instruments LabVIEW software.

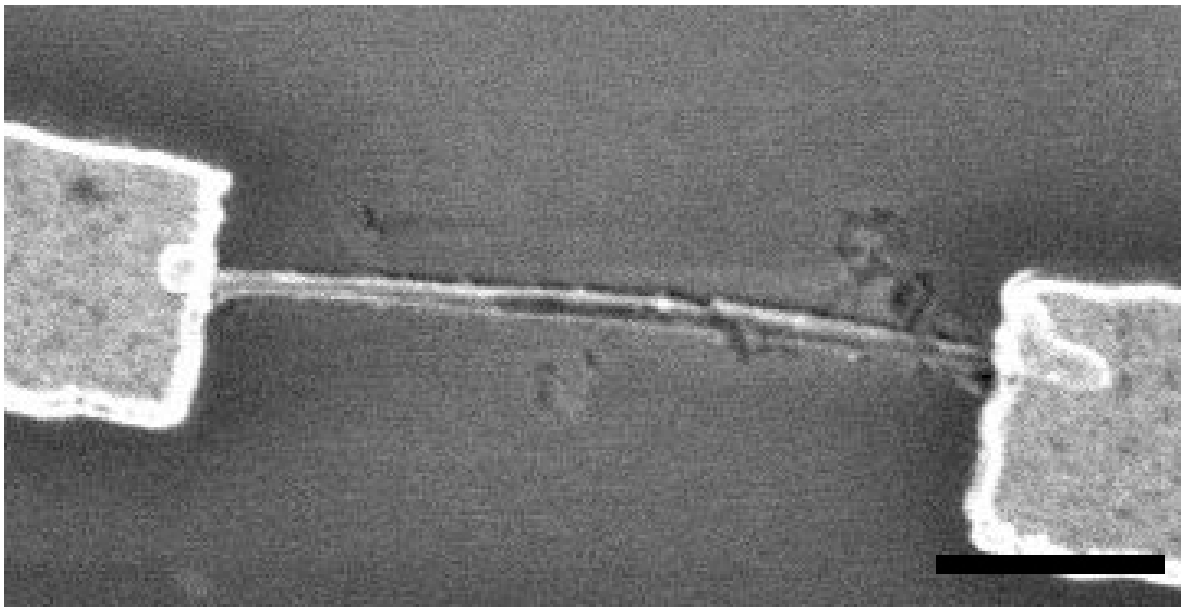

Figure 4.1: SEM image of a FET based on a heterostructured a Au-CdSe-Au nanowire. Scale bar is 1 μm. The darker section near the middle of the nanowire is composed of CdSe.

4.4 Results & Discussion

Figure 4.1 contains an SEM micrograph depicting the typical physical characteristics of a nanowire produced from the sequential electrodeposition of various materials from solution. These structures have mean lengths of 4.0 $\pm$0.22 μm and an average CdSe channel length of 1.1 μm $\pm$0.09 nm, which can be altered by varying the number of cycles performed during the CdSe electrodeposition step. The mean diameter of the nanostructures is 80 nm, which corresponds to the pore size as is defined by the PA template. Retrieval of useful properties about these FETs such as carrier mobility and the resistance of the nanowire is achieved by employing a technique recently outlined by Zhang et al.(Zhang et al., 2007a) Application of standard thermionic emission models alone underestimates the current across a reverse biased nanoscale Schottky

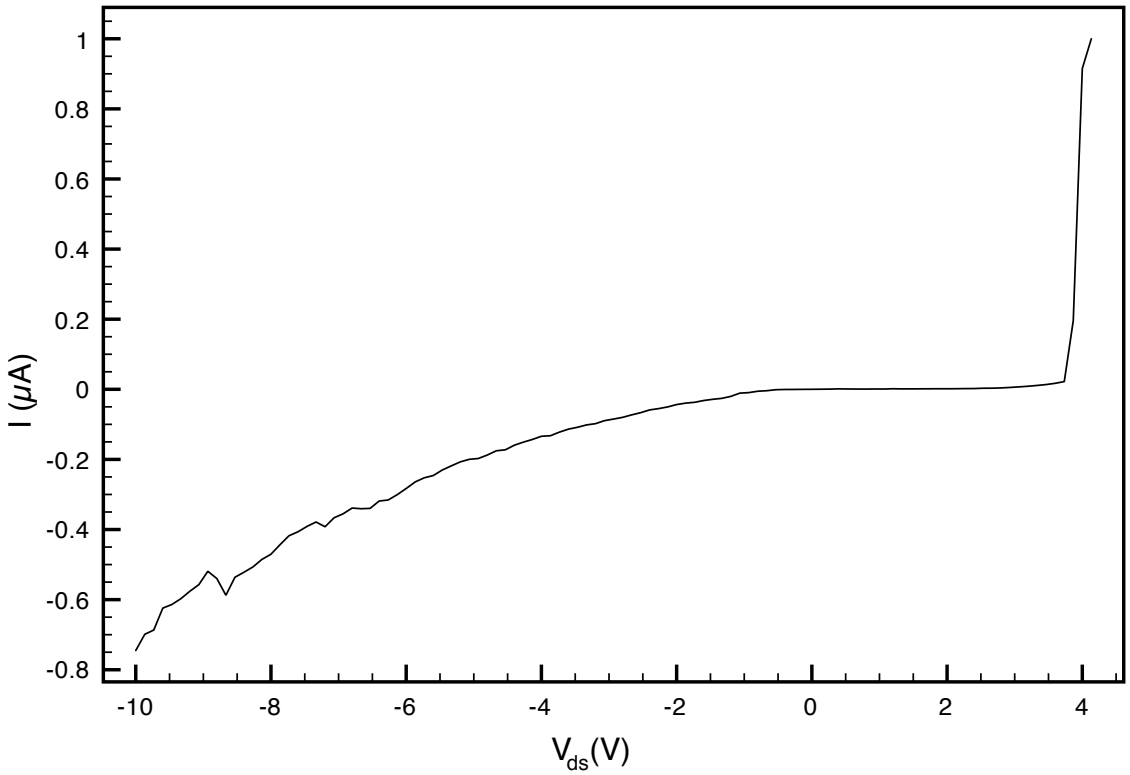

Figure 4.2: Experimental $I - V$ curves typical of heterostructured Au-CdSe-Au nanowires 80 nm in diameter with a 900 nm long semiconductor channel.

barrier(Zhang et al., 2006b) and therefore underestimates the mobility of the majority carriers. Thermionic emission is the most commonly used model for Schottky contacts and is thus used often when analyzing the forward-biased current of semiconductor nanowires.(Heo et al., 2004) The reverse-biased current, however, is underestimated and although this underestimation is negligible for microelectronic structures where the current saturation occurs at relatively low values, it becomes non-negligible for nanoelectronic structures since the device current is much smaller (10 nA). The analysis carried out here is based on thermionic field emission and adequately describes the tunneling effects of a reverse-biased junction, which dominates the reverse-biased

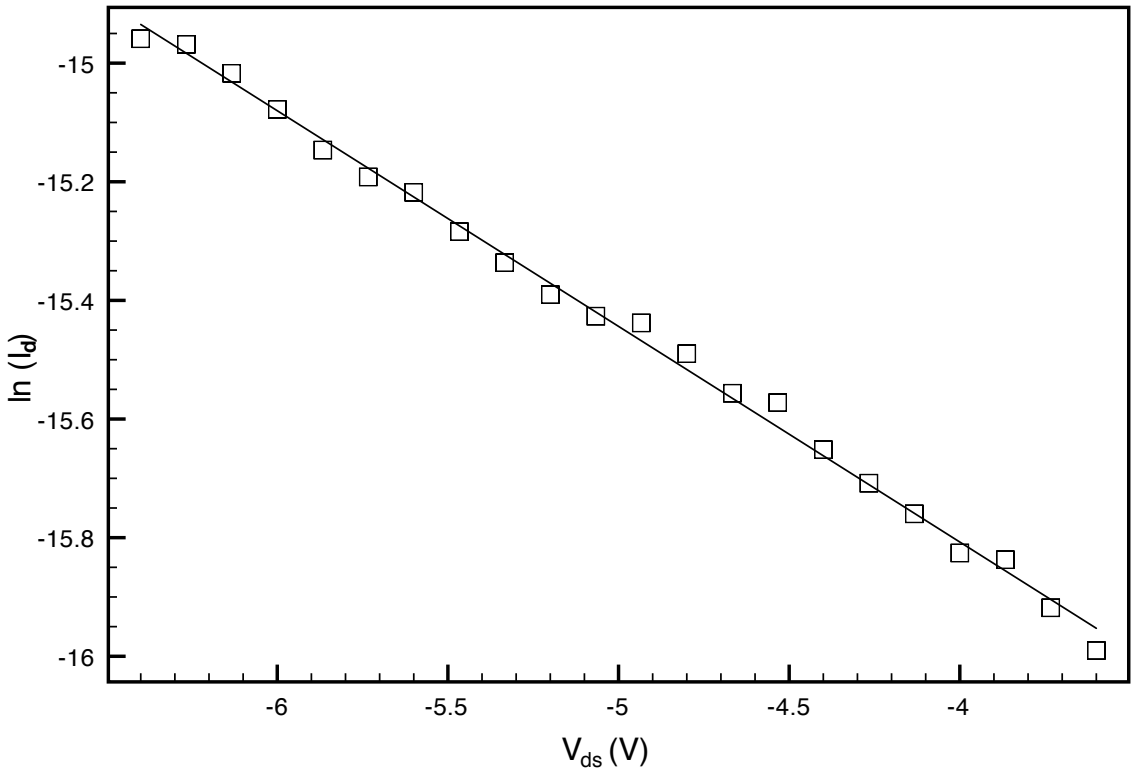

Figure 4.3: ln(I) vs V plots (experimental and fitted) derived from Figure 4.2 of heterostructured nanowires at intermediate bias.

current measured and explains the almost symmetric nature of the experimental $I-V$ curves. Figure 4.2 contains a typical experimental $I-V$ curve collected from an 80 nm heterostructured nanowire. The resistance of the nanowire was first extracted from the large bias portion of the curve using the differential voltage method(Zhang et al., 2006b) to obtain a value of 1.4± 0.3 MΩ cm^{-1} using the equation $R = a_{NW}(dV/dI)$ $\approx dV/dI$. We then focus on the intermediate biased regime of the $I-V$ curve, which can be described by equation 4.2 with the appropriate fitting parameters, in order to

obtain additional information by making use of the equation

$$lnI = ln(SJ) = ln(S) + V\left(\frac{q}{kT} - \frac{1}{E_0}\right) + lnJ_s \tag{4.7}$$

where S is the contact area of the Schottky barrier, J is the current density through this barrier, E_0 is a parameter that depends on the density of the majority carriers, and J_s is a slowly varying parameter based on the applied bias.(Zhang et al., 2006b) Figure 4.3 contains a plot of the current in this intermediate regime on a logarithmic scale plotted versus the applied voltage to yield a series of data points which can be fitted to a line of slope $q/(kT) - 1/E_0$. This can be used to obtain the parameter E_0, which we find to have a value of 46.7 meV and can be used to obtain the characteristic energy E_{00} through the relation(Horváth, 1996)

$$E_0 = E_{00}coth\left(\frac{qE_{00}}{kT}\right) \tag{4.8}$$

with

$$E_{00} = \frac{qh}{4\pi}\left[\frac{N_d}{m^*\epsilon_s\epsilon_0}\right]^{1/2}. \tag{4.9}$$

For comparison, the parameter E_0 was determined to have a value of 26.4 meV for heterostructured nanowires that were constructed without a graded interface between the last two electroplated metal and semiconductor segments.

The electron concentration N_d can be extracted from eqn. (4.9) and the electron mobility can be calculated from $\mu = 1/qn\rho$ where ρ is the resistivity of the heterostruc-

tured nanowire. Combining this information we obtain a value of 1.5±0.1 cm^3 V^{-1} s^{-1} for the electron mobility with the carrier concentration being 5.95 × 10^{18} cm^2. The electron mobility of the nanowire μ is typically calculated via the transconductance g_m for a given source-drain bias(Martel et al., 1998) via

$$\mu = \frac{g_m \times L^2}{C \times V_{sd}}, \tag{4.10}$$

where C can be estimated as the capacitance for a cylinder near an infinite plane

$$C = \frac{2\pi\epsilon L}{ln(2t/r)}, \tag{4.11}$$

and ϵ is the dielectric constant of the SiO_2, L is the channel length of the nanowire, t is the thickness of the oxide layer and r is the radius of the nanowire. Combining eqns. (4.10) and (4.11) and substituting the appropriate values we find $\mu = 0.49$ cm^2 V^{-1} s^{-1}, which is significantly less than the value derived above. The main difficulty with the infinite plane model is that it assumes the gate oxide fills the entire space surrounding the nanowire. This results in an overestimation of the backgate capacitance and a decrease in the inferred mobility.(Khanal et al., 2007) From the $I - V$ characteristics in Fig. 4.4, these heterostructured nanowires were found to have transconductances of ∼20 nS for V_{sd} of 1.0 V. The normalized transconductance (g_m/W) is found to be approximately ∼100 nS/μm using a channel width (W) of 200 nm, which is over an order of magnitude higher than those found in structures such as ZnO nanobelts(Arnold et al., 2003), but an order of magnitude less than high quality single-crystal ZnO

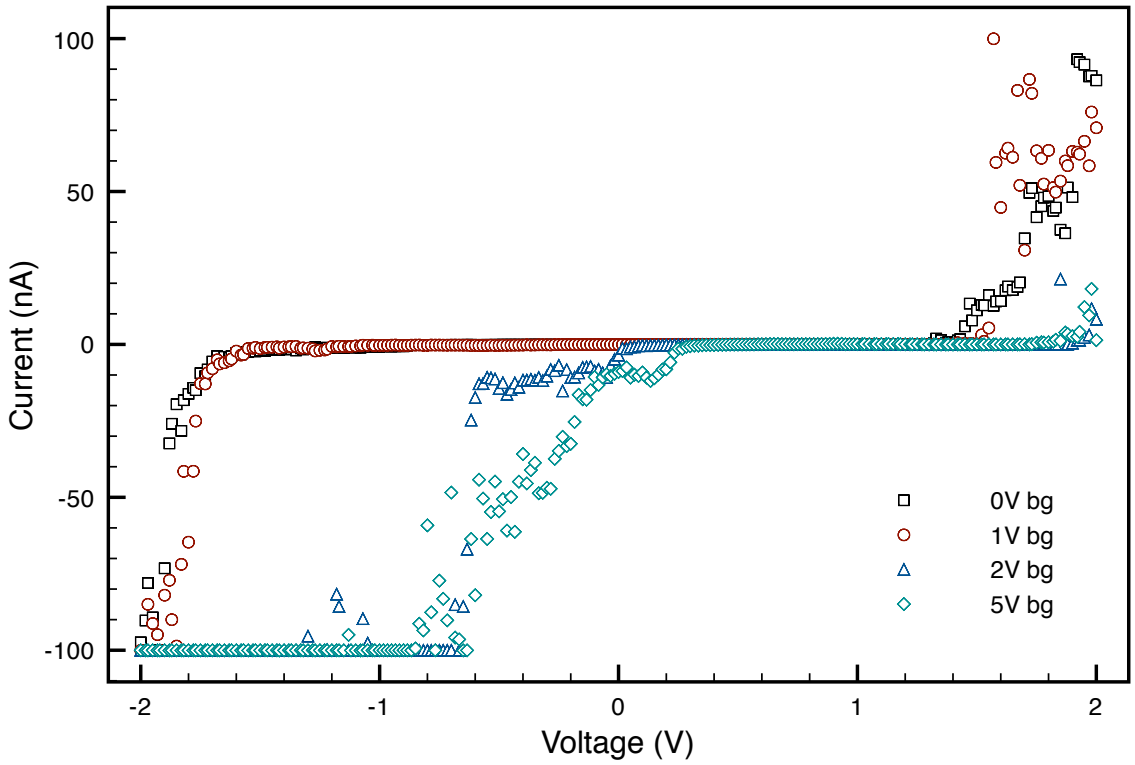

Figure 4.4: Experimental *I*-*V* data collected from 200 nm electrodeposited Au-CdSe-Au nanowires. The 'railed' curves for applied backgate voltages of 2 V and 5 V corresponds to the compliance limits on the Keithley.

FETs fabricated via catalyst-free metalorganic vapor phase epitaxy(Park et al., 2004b) which is believed to be fast enough for future use in applications requiring high speed electronics. For comparison, the mobilities found in more conventional Si based FETs are reported to have mobilities between 10 and 100 cm^2 V^{-1} s^{-1} for structures with channel widths of 10 nm.

Additionally, it is worth mentioning that Zhang et al. noted that an interfacial insulating layer between material interfaces may affect the tunneling current at very low bias.(Zhang et al., 2006b) Unlike typical nanowires where the metal/semiconductor

contacts are formed in the chamber of a thermal evaporator or with some other low pressure metal evaporation system, the ones constructed here are never introduced to ambient conditions as the contacts are formed *in situ*, and any effects from an insulating layer between material interfaces of the nanowire should be minimal. Also notable is that the increase in measured current of the nanowires based on the manner in which the electrochemical solutions are exchanged indicates that a graded interface formed by dithering the Au and CdSe materials in order to create a Au-doped CdSe region could be helpful in achieving the highest currents. This is much like previous methods employed in the creation of quantum cascade lasers constructed by metal organic vapor phase epitaxy, (Troccoli et al., 2005) where it was also found that not halting the growth process between material interfaces results in comparatively improved device performances(Troccoli et al., 2004).

Chapter 5

Mechanical properties of heterostructured nanowires

5.1 Introduction

Even though nanowires have gained significant attention as potential building blocks for larger nanoscale systems due to their interesting and widely varying mechanical and electrical properties, significantly less is known about the mechanical properties of individual structures although generally the composition and structure have been well cataloged.(Xu et al., 2000; Zhang et al., 2001) One of the main unknowns in assembling larger structures from these individual building blocks is the lack of sufficient information about how size and microstructure affect material properties such as the mechanical strength and electronic parameters, thus prompting researchers to investigate the relationship between structure and electromechanical properties. (Wu et al., 2006; Chu et al., 2002; Shao et al., 2004; Fan et al., 2004; Gao et al., 2005; Anthony et al., 2007; Lin et al., 2008)

In recent years, experiments have been performed on single material nanowires suspended and anchored above trenches defined by focused ion beam (FIB) milling of a silicon substrate.(Wu et al., 2005; Wu et al., 2006) The mechanical properties of these suspended nanowires were investigated by atomic force microscopy (AFM), and it was determined that small diameter gold nanowires have a Young's modulus slightly lower than the values found in the bulk material. Since then, others have also performed measurements on nanowires composed of differing materials with similar diameters but using different methods to extract similar values.(Li et al., 2007) One particularly attractive aspect of the AFM lateral bending system devised by Boland is that the entire spectrum of mechanical properties can be probed, unlike other methods which only explore a subset of these properties.(Li et al., 2007; Wong et al., 1997; Falvo et al., 1997) However, to date no one has probed more complex heterostructured metal-semiconductor-metal nanowires to determine standard mechanical properties including the Young's modulus, yield and failure points, nor have they explored how these nanowires may be strengthened mechanically in order to improve the values associated with the yield and failure points, which will have a direct impact on the failure rate of electronic systems composed of these structures due to mechanical stress. Given the plethora of information obtainable from this technique, a modified version of this method is used here to determine the Young's modulus of heterostructured nanowires. This report determines the Young's modulus, plastic modulus, yield and failure points of heterostructured metal-semiconductor-metal nanowires fabricated by electrochemical deposition and compares the values determined for structures fabricated through simple

solution exchange with structures that have a graded interface between the metal and semiconductor sections. Preliminary results indicate that control of microstructure is not only effective in controlling the mechanical properties of single material nanowires but may also be effective in controlling the mechanical properties of heterostructured nanowires as well.

5.1.1 Scanning Probe Microscopy Background

When most people think of microscopes, the picture that typically comes to mind is one that uses focused electromagnetic radiation in order to produce a magnified image of the sample of interest. Historically this radiation was first in the form of photons and then progressed to electrons - both of which can provide images of the surface of a sample. Optical microscopes can easily generate images magnified 10,000x and for electron microscopes in excess of 100,000x with 30 nm resolution or less.

One limitation of microscopes that use electromagnetic radiation in the visible light spectrum is that only one plane of the surface being imaged is in focus at any one time. With the exception of differential confocal microscopy, which can provide resolutions in z down to several nanometers,(Zhao et al., 2004a) very little information is available about the vertical dimensions of the sample under investigation with sub-nanometer resolution. Scanning probe microscopy (SPM) was developed as a desire both to address the vertical resolution limitations of traditional optical microscopy as well as to address the need to obtain images of higher resolution.

Scanning tunneling microscopy (STM) was the result of research conducted by Gerd

Binning and Heinrich Rohrer at IBM,(Binning et al., 1982) and is the 'grandfather' technology of all SPM methods in use today. Their work utilized methods first demonstrated by Young's surface profiler created in 1971,(Young et al., 1972) and operate on the principle that a sharp tip with an applied bias in very close proximity (1 nm or less) to a conducting or semiconducting substrate will produce a tunneling current between the probe tip and the sample itself. The current produced across the 1 nm gap between the substrate and the tip will vary with the distance between the tip and the sample, and is used to create an image of the surface. Due to the exponential relationship between the tunneling current and the distance between the tip and the sample, STMs have atomic resolution laterally and sub-angstrom resolution vertically.

One limitation with STMs is that due to the requirement of a tunneling current to produce an image which rules out the possibility of imaging insulating samples. AFMs address this limitation by rapidly oscillating a sharp tip attached to the end of a cantilever over a surface, and this concept was first demonstrated by Wickramsinghe in 1987 based on a suggestion in a 1986 paper written by Binning and Quate(Binnig et al., 1986) who noted their non-vibrating AFM could be improved by vibrating the cantilever above the surface of the sample being scanned. The deflection of the cantilever as it is rasterized over the sample is measured by monitoring the position of a focused beam of light on a photodiode that is bounced off the back of the cantilever as it scans the sample, and allows a computer to produce an image of the topography of the sample. Because there is no dependence on a tunneling current, insulators as well as semiconductors and conductors can be imaged.

More specifically, attractive and repulsive forces between the sample and the scanning tip results in deflection of the tip in response due to electrostatic forces. One of these forces is an interatomic force known as the van der Waals force and has a dependence on the distance between the tip and the sample. When the distance between the tip and the sample is 1 to several tens of nanometers the van der Waals force is attractive largely as a result of the long range aspects of this force. Images of a sample acquired within this range of distances is often referred to as 'non-contact' imaging. When the distance between the tip and sample is less than 1 nm, a repulsive force is experienced by the tip and is considered the 'contact' regime of imaging. Contact mode can be used for the manipulation of a sample, while non-contact or intermittent-contact mode is used as a non-destructive imaging mode.

Since the initial development of the AFM, many other scanning microscopy methods have been derived from the basic AFM technique that can be used to examine various aspects of a material's surface with nanometer or better resolution. For example, magnetic force microscopy (MFM) is available when a thin ferromagnetic film (or any other ferromagnetic nanostructure(Yang et al., 2005)) is applied to a tip, and a spatial image map spatial is collected based on differences in the magnetic field of a sample and the distance between the sample and the tip. This method can be used, for example, to image 'standard' magnetic samples or to determine the location of magnetic particles in a non-magnetic film(Clendenning and Manners, 2004). Lateral force microscopy can be used to determine information about the friction of a surface. This method of microscopy gains information through the twisting of the cantilever as it interacts with

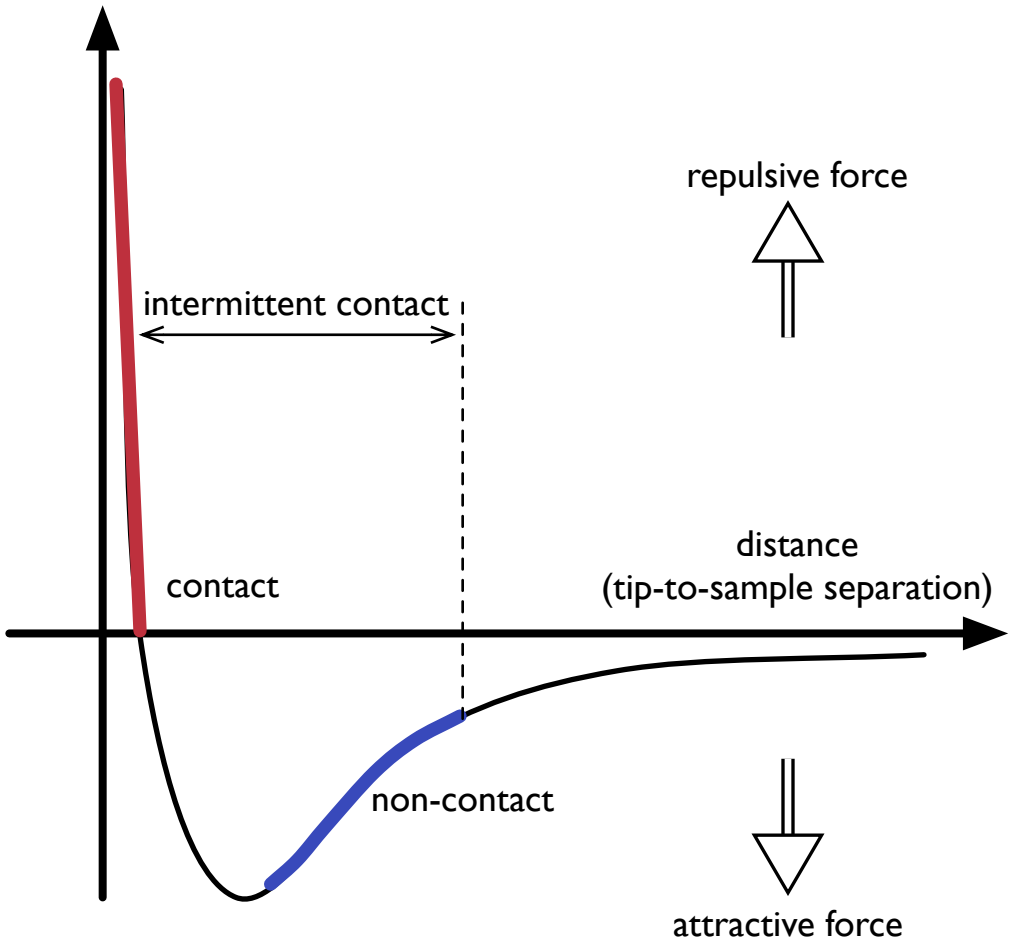

Figure 5.1: Interatomic force vs. distance curve.

the surface, which produces a horizontal translation of the laser spot on the photo-quadrant diode.(Schwarz et al., 1996; Liu et al., 2001) To decouple the changes in the lateral force signal due to friction versus those due to topographical edge effects, both image maps should be collected at the same time to aid in deconvolution. Phase microscopy collects information about the phase lag between the signal used to oscillate the cantilever and the output response of the cantilever due to interactions between the

driven tip/cantilever system and interactions between it and the surface being scanned. This information can be collected while imaging in a mode such a non-contact mode or during MFM and can be used to determine differences in material properties such as elasticity and friction.(Stark et al., 2001)

The imaging methods used to perform the mechanical manipulations here only made use of the non-contact imaging mode for direct imaging of the sample to be manipulated, and contact mode for the actual manipulations performed on suspended structures.

5.2 Experimental

The experiments performed here are similar in execution to previous experiments on the mechanics of suspended nanowires.(Wu et al., 2005) The main difference in the process used here is the definition of trenches *after* well dispersed nanowires are deposited on the substrate, which was chosen because nanowires can be individually selected and relatively oriented to the underlying defined pits for optimal manipulation. Previous methods have relied on nanowires to come to a final resting place above a predefined trench on the patterned substrate.

One particularly troublesome aspect of depositing nanowires onto any substrate is the constant aggregation that occurs when deposited at room temperature conditions. Figure 5.2 contains an example of how extreme the aggregation can be when deposited in an uncontrolled manner. The aggregation normally observed in deposited nanowires

was virtually eliminated by making use of a previously devised deposition method that yields well dispersed samples across a substrate.(Lee et al., 2007) For comparison, figure 5.3 contains the results of a typical deposition after a hot plate was set to 160 C and a 4 μL drop was placed on top of a patterned silicon/silicon dioxide wafer within an area of interest. Pits beneath individual nanowires were formed by defining windows in a poly(methyl methacrylate) (PMMA) resist and then using the patterned layer as a mask for etching the underlying silicon oxide with hydrofluoric acid. The PMMA itself was left on the substrate after patterned etching of the silicon oxide layer and served as anchors to pin down the nanowires over the defined pits, which were typically 1.2-1.5μ wide and 400-800 nm deep. The heterostructured nanowires were synthesized in porous aluminum (PA) templates based on previous methods.(Skinner et al., 2006)

Successful manipulations were performed on suspended structures via application of a lateral force with an AFM tip using commercially available software known as the Nanomanipulator to control the position of the tip.(Taylor, 1991) In a typical experiment, an image of the structure to be manipulated was first acquired in tapping mode followed by precise positioning of the tip several hundred nanometers below the bottom of the suspended nanowire via a six degree of freedom haptic controller. Lateral forces were then applied by repeatedly stepping the tip 1-5 nm per step along a predefined direction towards the nanowire until contact was made by monitoring the lateral force signal as determined by the photodiode. *F-d* curves were captured by the software. A portion of the curve is always collected away from the nanowire itself in order to determine a baseline which is then used as the reference for zero applied lateral force

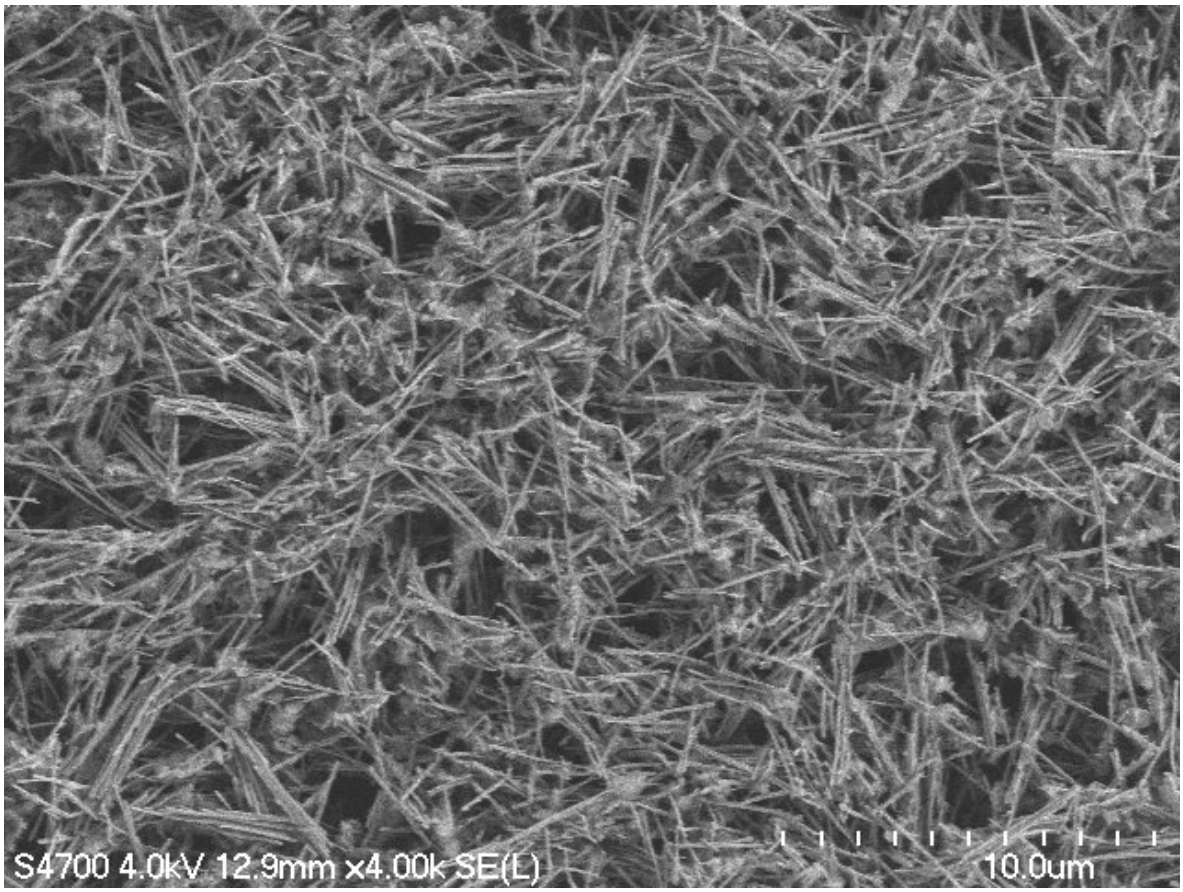

Figure 5.2: Densely aggregated nanowires at a concentration of ~4×10^8 per μL deposited at room temperature conditions from an ethanol solution.

and ensures that forces associated with deformation of the nanowire is entirely due to loading of the nanowire itself. It is worth emphasizing that closed loop control of the z-position of the nanowire is achieved in software by definition of the X-Y plane in what is known as 'direct-step' mode. This method of manipulation provides well defined movements along any given axis of an arbitrarily chosen coordinate system and prevents the tip from ever coming into contact with the bottom of the trench since the X-Y plane is chosen to be parallel with the surface of the sample itself.

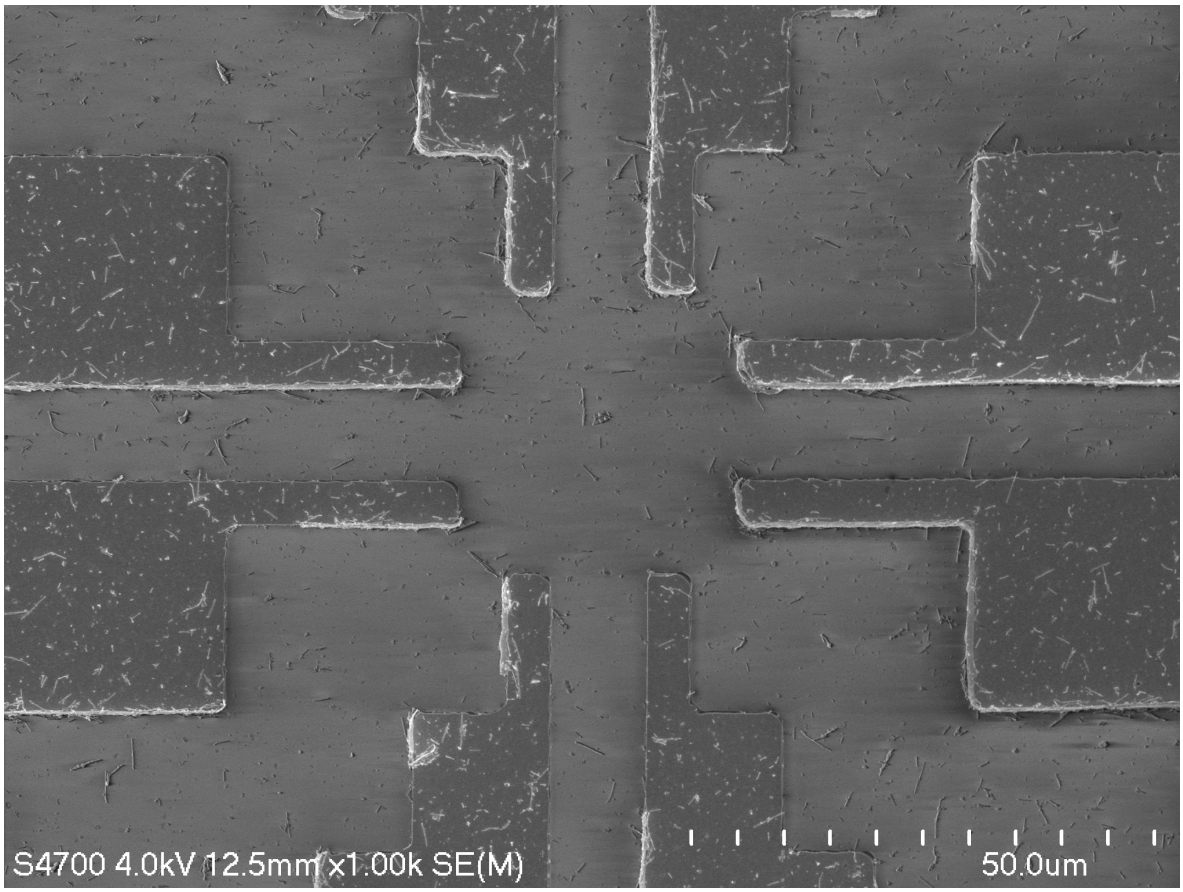

Figure 5.3: Dispersed nanowires from the same sample as those deposited in figure 5.2 deposited from a 4 μL drop of ethanol onto a hot plate set to 160 C.

5.2.1 Sample preparation

Heterostructured nanowires were constructed in porous alumina templates obtained from Synkera Technologies. Nanowires were constructed by sequential deposition of gold, silver and cadmium selenide into templates previously prepared for electrodeposition containing 80 nm pores. Silver (1025) and gold (Orotemp 24) baths were both obtained from Technic, Inc. Silver was thermally evaporated onto one side of the template in sufficient quantities to form a continuous film over the previously exposed pores. The prepared templates were submerged in N,N-dimethylformamide for 30 mins and

briefly agitated in an ultra-sonicator bath before being submerged in the electrodeposition bath to aid in pore wetting. After deposition of the final Au segment, templates were rinsed repeatedly in distilled water before the thermally evaporated and electrochemically deposited silver was removed with a 6M HNO_3 solution. Free nanowires were obtained by submerging the template into 3M NaOH for 30 mins, followed by rinsing 3x with distilled water and centrifugation before being suspended in ethanol. Highly dispersed nanowires were deposited on photolithographically patterned silicon substrates with a 1 μm thick SiO_2 layer by dropping a 4 μL sample of nanowires onto a substrate heated to 160 C as described at the beginning of this section. Windows in PMMA were constructed over individual nanowires via electron-beam lithography and pits were formed beneath them by using the resist as a mask while etching select regions of silicon oxide with HF in order to create suspended structures.(Hall et al., 2007)

5.2.2 AFM cantilever calibration

Cantilevers with rectangular dimensions (Olympus) with normal spring constants between 0.8 and 2.7 N m^{-1} (70 kHZ) were used for manipulating suspended heterostructured nanowires. For lateral force calculations, the beam spot of the laser is assumed to be circular, and the response of the photodiode signal due to changes in vertical bending or lateral torsion of the cantilever is assumed to be equivalent. The lateral spring constant was obtained by obtaining force curves on a silicon surface and extracting the lateral spring constant from a beam bending model by supplying the appropri-

ate parameters for the normal spring constant and the cantilever geometry. Torsional constants ranged from 120 to 280 N m^{-1}.

5.2.3 Mechanical measurements on heterostructured nanowires

A microscope running the Nanomanipulator package(Guthold et al., 1999) was employed for mechanical measurements of heterostructured nanowires. The Nanomanipulator is a graphics interface designed to interact with an AFM. The topographic data are rendered in real-time as a three dimensional directionally illuminated image. The data are also coupled to a haptic interface which allows for interpretation via tactile feedback and aids in precise positioning of the tip, and was used to place the tip in the general vicinity of where a manipulation was to be performed. Manipulation of the nanowire was performed in 'direct-z' mode. This mode of the software allows the tip to be moved in a predetermined direction at a predefined height above the sample, and was used to perform manipulations on heterostructured nanowires suspended above chemically etched trenches.

5.3 Results and Discussion

Figure 5.4 depicts the typical layout of a suspended nanowire over a pit defined by electron beam lithography and chemical etching. The structures are located by scanning a large area of the sample (usually on the order of 100 μm^2) and then progressively reducing the scan area while keeping feature of interest in the center of the

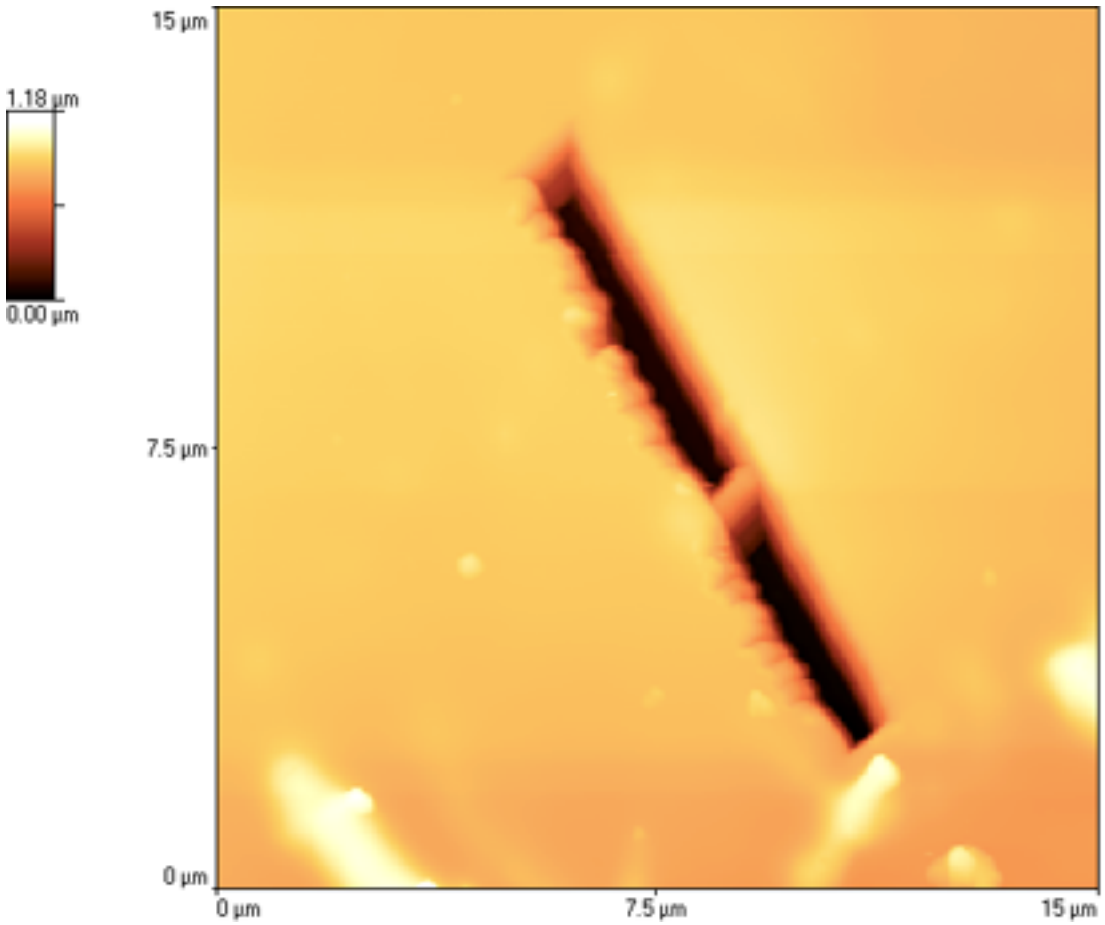

Figure 5.4: A heterostructured Au-CdSe-Au nanowire 80 nm in diameter suspended above a chemically etched pit under with its ends anchored by a PMMA overlayer. This image was acquired via AFM before any AFM manipulations were performed in contact mode.

scanning area. This progressive reduction in scan area is time consuming but important because of the lack of a closed loop x-y scanner on the AFM. As is apparent from figure 5.4, nanowires selected for manipulation are generally selected based on how isolated intact heterostructures are relative to other nanowires on the surface. Although a non-negligible number of the nanowires break during processing before the lithography stage commences, enough of the structures remain intact that it is not uncommon to often find a dozen or more intact within any randomly chosen 100 μm^2 area at the

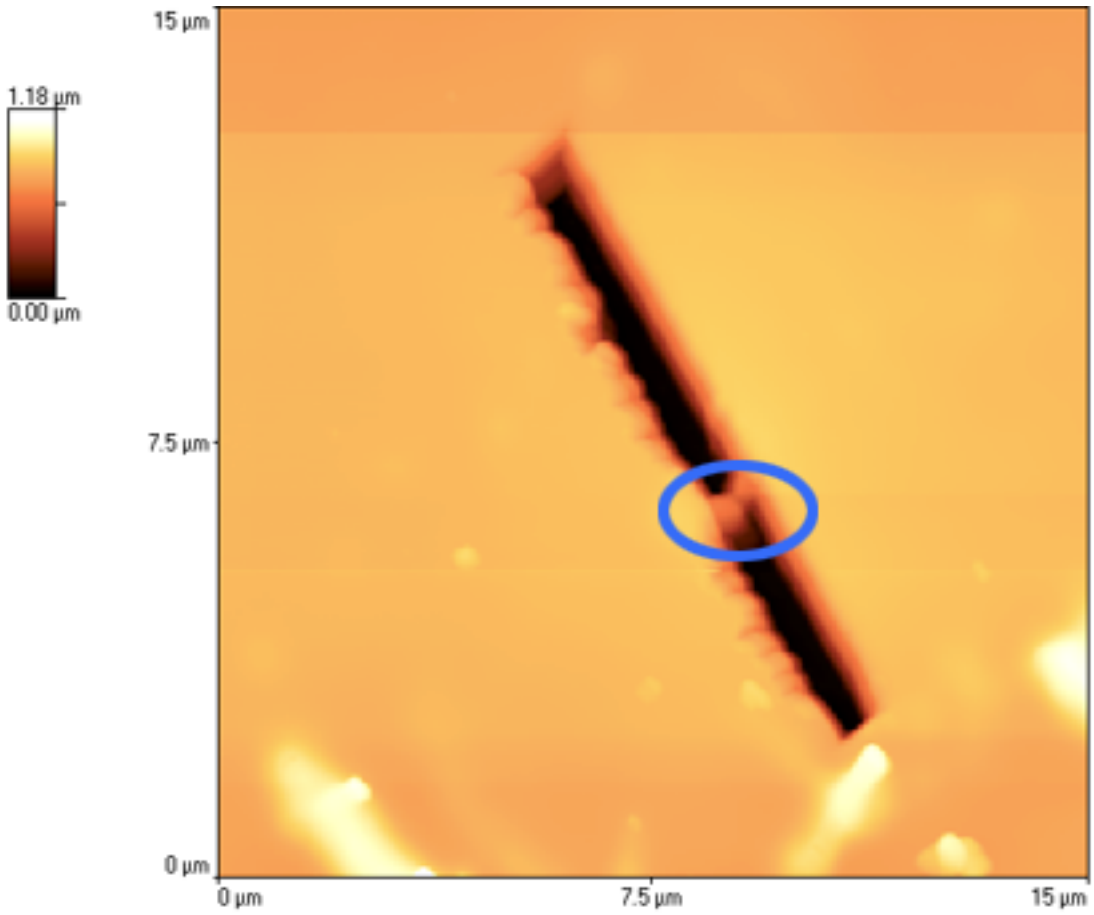

Figure 5.5: A heterostructured Au-CdSe-Au nanowire 80 nm in diameter suspended above a chemically etched pit under with its ends anchored by a PMMA overlayer. This image was acquired via AFM after AFM manipulations were performed in contact mode. The blue circle indicates where the break occurred in nanowire.

concentrations of nanowires in solution specified above.

Before manipulations are performed on any potentially suspended nanowire structure, height analysis is performed on the structure of interest beforehand. Figure 5.6 shows typical results presented when a structure is successfully suspended. Two lines are first drawn across the lithographically and chemically defined pit; one across the nanowire traversing the pit and the other across the pit without the nanowire. Two

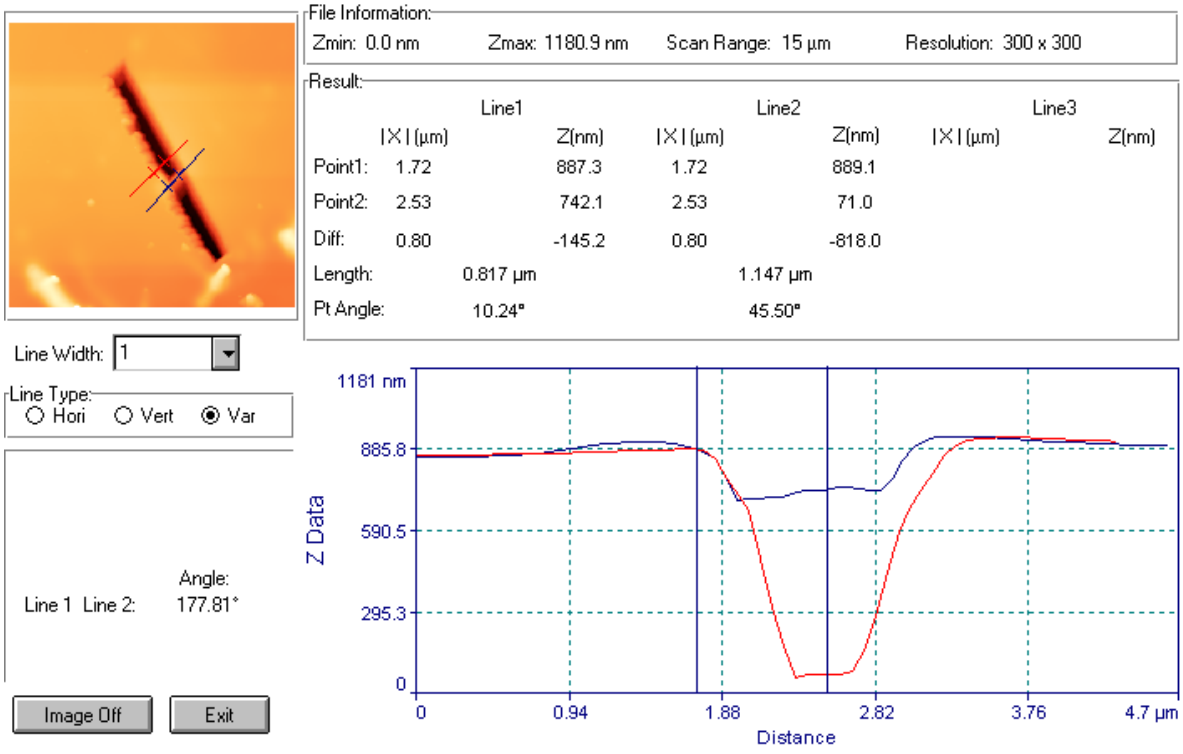

Figure 5.6: AFM height analysis of a suspended nanowire structure to determine if the structure is actually suspended or not. The difference in z between on Line 2 between points 1 and 2 in conjunction with the diameter of the nanowire indicate that this structure is indeed suspended.

lines are required because the line selected across the pit without the nanowire present measures the height difference between the bottom of the defined pit and the top of the PMMA, which includes the PMMA layer plus the diameter of the nanowire. To decouple the thickness of the PMMA from this measurements, which typically measures one to two hundred nanometers in thickness, a second profile is acquired across the pit across the including only the top of nanowire and the PMMA. Using the height of this line, along with the known diameter of the nanowire (approximately 80 nm for these nanowires), the true height of the suspended structure can be obtained. In figure 5.6,

this height is slightly more than 700 nm. Thus, the structure is suspended and can be safely used for manipulation without worrying about possible contributions from the bottom of the pit.

Manipulations are then performed by orienting the axis of the manipulation coordinate system by choosing the x-y plane to coincide with the surface of the sample itself, and x-axis is chosen to run parallel to the length of the pit the nanowire is suspended over. The tip of the AFM is placed within the pit away from the sample, and the z-position of the tip is set to be several nanowire diameters below the top of the suspended nanowire, but several hundred nanometers above the bottom of the pit itself. This chosen height along the z-axis in conjunction with the carefully selected orientation of the x-y axis allows steps of arbitrary sizes to be taken both approaching towards and receding away from the suspended nanowire. This creates the opportunity to gradually load, approach and remove arbitrary forces on the suspended structure, and allows for the investigation of both the elastic and plastic responses of the nanowire during the breaking tests. The stepping increment of the tip was typically chosen to be between 1 and 5 nm per step, and the direction of the tip path was always chosen to be perpendicular to the lengthwise orientation of the suspended structure. Most often this traversal direction of the tip was not perpendicular to the lengthwise orientation of the cantilever itself, and the relative angle between the cantilever and the direction of the manipulation was accounted for when calculating the lateral forces applied to the suspended structures.

Typical $F - d$ curves collected by recording the signal originating from the pho-

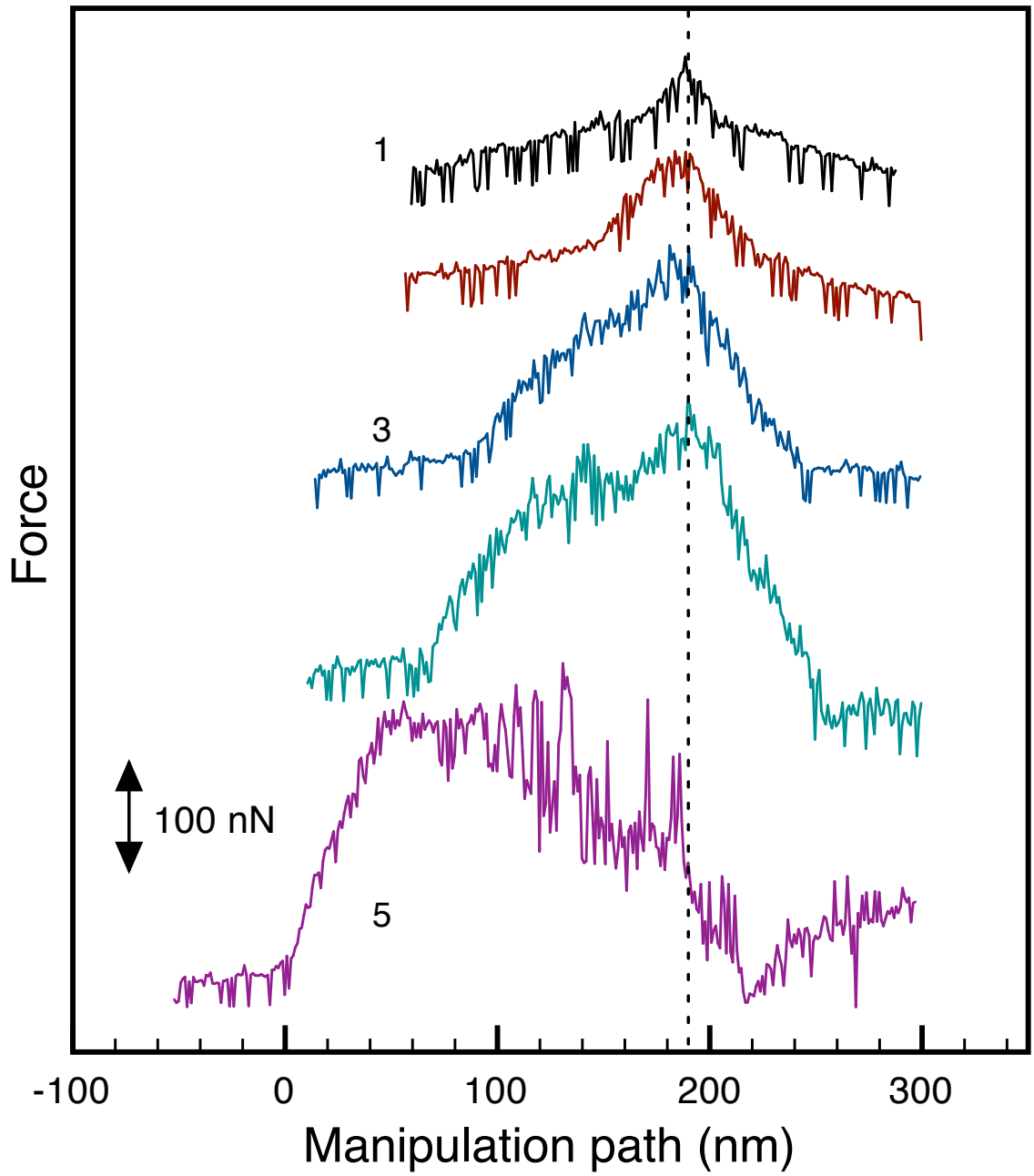

Figure 5.7: $F - d$ **curves collected during consecutive manipulations of a single suspended nanowire via an AFM tip. Vertical line represents reversal point of the trajectory of the AFM during the manipulation. Numbers represent manipulation number.**

todiode and recording the lateral component during the consecutive manipulations performed for breaking tests are presented in Figure 5.7. The numbers correspond to the approach number of the AFM tip during successive manipulations of the same nanowire, and the dashed vertical line denotes the point along the manipulation path at which the direction of manipulation was reversed. The spikes present in are noise from the photodiode and is unfortunately difficult to remove from the raw data signal. Although it can be removed via post-processing, It has been left here for completeness as it does not detract from the overall shape (that is, the slope) of the $F - d$ curves. Curve 1 shows that under small loads, the wire responds with linear displacement as the response is initially elastic in this regime. With successively increasing loads, the wire begins to undergo plastic deformation which is apparent from the two different regimes of response as is determined by the two different slopes. It is also evident from this figure that the force is essentially constant during the initial approach of the cantilever towards the suspended structure. As force on the nanowire is decreased by reversing the direction and stepping the AFM away, the force decreases linearly which indicates the elastic response of the suspended system. Plastic deformation is not induced in curve 1, which is evident from the symmetry present in the overall shape of the $F - d$ trace during both the approach and the reverse approach of the AFM tip-cantilever system.

Increased loading of the suspended nanowire ultimately results in plastic, non-reversible deformation of the nanowire structure. Curves 2 - 5 of figure 5.7 each display two distinct slopes during the forward trajectory of the AFM tip as the suspended

nanowire system is loaded with a force. The kink along the $F - d$ curve between the initial and subsequent slopes indicates the yield point where nanowire deformation changes from the elastic to the plastic regime. At this point in the curve, deformation requires less force and becomes easier. In figure 5.9, the failure point marked in the diagram denotes the point where the entire structure breaks into two, and subsequent AFM images of the suspended structure results in images like the one in figure 5.8.

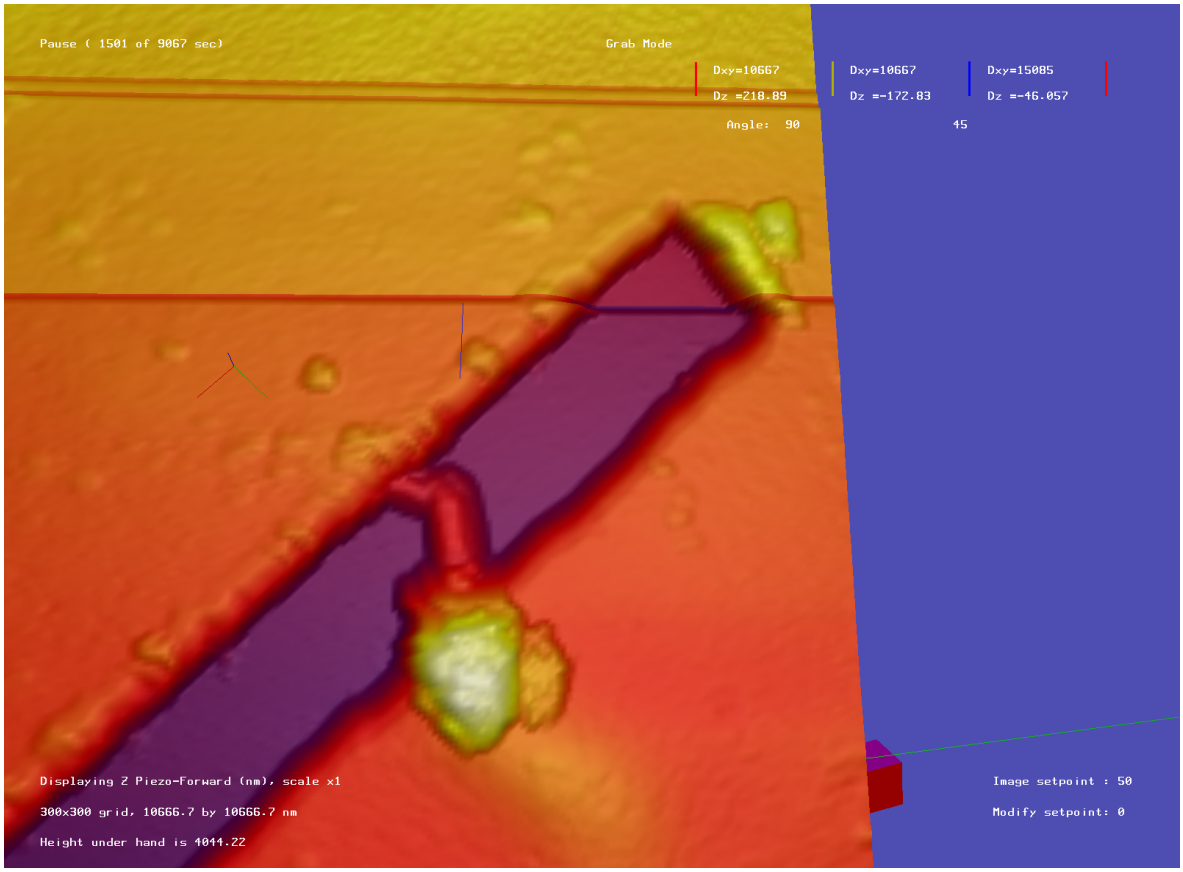

Figure 5.8: Suspended heterostructured nanowire after deformation beyond its point of failure. Image acquired through the Nanomanipulator software.

The initial linear portion of the $F - d$ curves adhere to the criteria for elastic beam-bending theory, and can be further examined to determine mechanical properties

about the suspend heterostructured nanowire system. From ref (Gere and Timoshenko, 1990) the relationship between the Young's Modulus E and the elastic deformation of a cylindrical beam at its midpoint is given by

$$E = \frac{FL^3}{192dI} \tag{5.1}$$

where F is the lateral force, L is the length of the suspended beam, and I is the moment of inertia of the cylinder with radius r, given by $I{=}(\pi r^4)/4$. It is also well known(Schwarz et al., 1996) that the lateral force F produced by a rectangular silicon cantilever of length L_c, with dimensions of thickness t and width w is related to the signal ΔU_{lat} (nA) measured by a photodiode via

$$F = \left(\frac{Gwt^3}{2L_c^2 l}\right)\left(\frac{1}{S_{ver}}\right)\Delta U_{lat}. \tag{5.2}$$

Here, G is the shear modulus of silicon and l is the length of the tip. S_{ver} is the vertical sensitivity, and is determined by $F - d$ curves. It is worth mentioning in equation 5.2 that the factor of 2 in the denominator replaces the usual factor of 4 found in other versions of this equation. This extra factor of 2 occurs because others calculate the signal U_{lat} by scanning the tip back and forth in a 'friction loop' to determine the change in the $L - R$ (left minus right) signals measured by the photodiode when determining ΔU_{lat}, as it is a measure of the change in the deflection of the cantilever not from the normal axis of the cantilever at rest but the deflection from the forward scan of the friction loop to the reverse scan. We often make the assumption that the response of

the photodiode in the vertical and lateral direction is symmetric (i.e. the laser spot on the photodiode is a perfect circle and not an asymmetric ellipsoid). Thus the deflection in the determination of the vertical sensitivity only involves the deflection away from the normal axis when taking the initial force curves, and the extra factor of two is not needed. The dimensions of the AFM tips and cantilevers have been previously been determined by SEM, and have been consistently found to be well correlated with the dimensions reported by the manufacturer. In addition to obtaining values for E, the yield strength can be calculated from the yield force, which corresponds to the point on the $F - d$ curves between the elastic and plastic regimes, using the equation(Gere and Timoshenko, 1990)

$$\sigma_y = \frac{F_y L}{2\pi r^3}. \tag{5.3}$$

For the $F - d$ curves presented above, the yield strength is found to be 130 MPa, which is substantially less than the 3.5 - 5.6 GPa values reported for Au nanowires.(Wu et al., 2005) Additionally, the Young's modulus for these suspended structures was found to be 17$\pm$11 GPa, which is also much less than then 70$\pm$11 GPa values reported. These significantly smaller values suggest that the junction between the CdSe semiconductor, which is a ceramic, and the metal segment of the nanowire is the weakest link of the structure.

One curiosity that repeatedly showed up in multiple experiments performed on different suspended heterostructured nanowires all derived from the same batch of nanowires was the increase in the elastic response as successive manipulations were

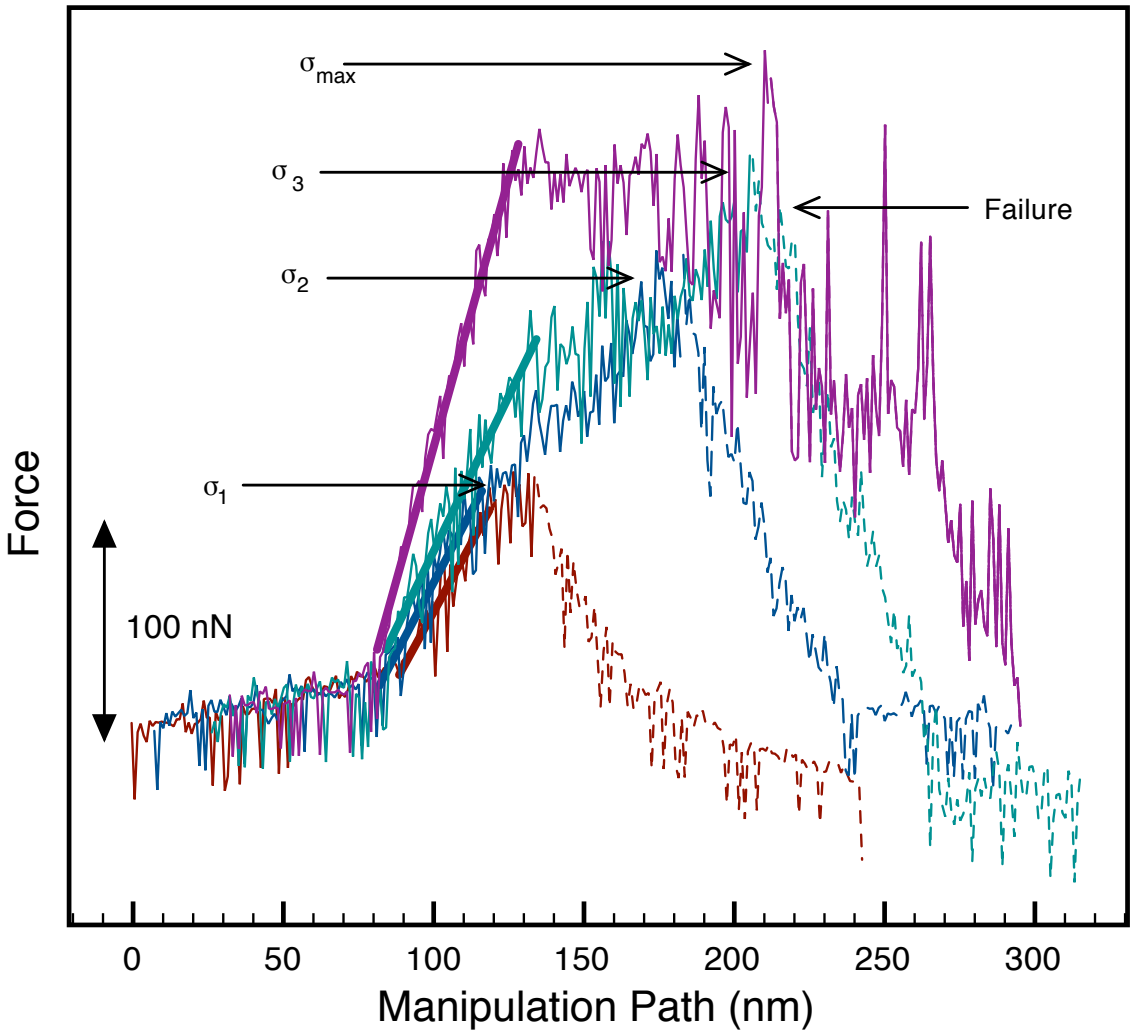

Figure 5.9: Successive $F - d$ curves collected during plastic deformations on a single suspended heterostructured nanowire. Bold lines are fitted for the elastic portion of each underlying curve.

performed. In figure 5.7, the first four curves have an average Young's modulus of 11.3±0.6 GPa, but this value doubles to 22.5 GPa by the 6th and final manipulation performed. (First manipulation omitted in figure 5.7 for clarity.) This gradual increase in the modulus is more apparent in figure 5.9, which compares the relative shapes of the $F - d$ curves after consecutive manipulations. The progressive increase in the Young's modulus may be the result of work hardening at the metal-semiconductor interface, and may be similar in origin to effects seen in other nanostructured materials.(Wu et al., 2006) Further investigation is required to determine the cause of this increase in E due to repeated loading and unloading of the suspended structure.

Chapter 6

Summary and future directions

6.1 Research summary and significance

This thesis has evaluated data collected from mechanical deformation and electrical measurement experiments of heterostructured metal-semiconductor-metal nanowires. These data provide clues as to how these devices compare to silicon structures, as well as information about their mechanical robustness. It has also been demonstrated that these and similar composite structures can be functionalized arbitrarily along its longitudinal axis with self-assembled monolayers such as DNA. This opens the door for the attachment of this structure to other predetermined locations via DNA hybridization.

Due to the need of nanoscopic current carrying structures, the feasibility of producing structures that may fit this need for future electronics applications was first examined to determine how much control could be gained over the physical aspects of these structures (Chapter 3). It was discovered that electroless deposition routes produced structures with rough surfaces and little to no control over the overall lengths. It was also found to be an inefficient method in terms of time. Comparatively, elec-

trochemical deposition routes showed that fine control over both the lengths and the diameters could be produced quickly. Electroless deposition methods may have their place in the formation of interconnects between devices, but for the construction of the devices themselves electrochemical deposition is much more useful.

Next, exploitation of the chemical and thermal robustness of the template presented the opportunity to attach different types of bifunctional modifiers including self-assembled monolayers and DNA to arbitrary segments along the length of and at the ends of these nanowires. It was demonstrated that a heterostructured nanowire could be used as the substrate for the attachment of these molecules or a substrate composed of a single material could be used as well. This result is important because the excessively small nature of the structures produced along with the sheer number of structures produced at once make it impractical to employ conventional lithographic methods to assemble working devices from these structures. This functionalization method provides a route towards the directed self-assembly of larger functional structures that require devices to be placed with specific orientations at specific locations.

The electrical properties of these structures were then investigated by collecting standard $I - V$ curves using a two terminal setup (Chapter 4) and a quantitative parameter retrieval method. A quantitative method was used to calculate values for the mobilities of majority carriers in the device instead of determining these values from the more often used combination of the transconductance and cylinder near an infinite plane model due to the underestimation of this value from the latter method. It was found that these mobilities could be increased threefold by creating a graded interface between

the metal and semiconductor segments of the heterostructured device. This finding should be useful for heterostructured devices composed of different semiconductors where the highest possibility mobilities are desired for electronics applications.

The mechanical properties of these structures were also investigated to determine their elastic and plastic response under an applied load (Chapter 5). A scheme was devised to construct a platform that would reliably produce suspended nanowire structures that could then be manipulated with an AFM tip. It was found that even though the suspended nanowires are composed of a ceramic semiconductor and a metal that has undergone considerable investigation, the yield strength and Young's modulus for these structure is considerably lower than values previously reported, suggesting the junction is the weak point of the entire structure. Future fabrication schemes for similarly structured devices may wish to investigate methods of strengthening this junction.

6.2 Future research directions

Although a broad range of topics have been addressed here, there are still plenty of areas that demand further attention. The first and obvious area begs further study is improving the mechanical robustness of these heterostructured nanowires. While the values obtained thus far are not disastrous, improvements in physical stability are always welcomed and in particular it would be wonderful to discover a way to reduce the number of nanowires that break during the washing step that occurs before the devices are placed on a substrate for electrical or mechanical measurements. One could imagine

that similar misfortune may be bestowed upon devices that are used in self-assembly processes, and as such would drastically reduce the yield of more complex structures that are complete and functional. The electrical conductivity of intact devices with respect to mechanical deformations would also be useful information to have, as it would provide a bound on the amount of strain a component in a larger system could undergo while potentially still remaining cohesive enough to remain functional.

Since the fabrication of structures such as these was first initiated back in 2004, a plethora of materials can now be electroplated into porous alumina templates, and as such new materials should be investigated to provide optimal electrical characteristics for the applications at hand. For example, it's well known that ZnO is excellent for high speed applications since the majority carriers in these devices tend to have relatively high mobilities, and a material such as this would be a logical candidate for future functional devices.

Another area requiring immediate attention is the integration of nanowires (both 'plain', single material nanowires and heterostructured nanowires) into larger, predictable structures. DNA lattices are now produced routinely by Chris Dwyer at Duke University and by others throughout the nation. The devices constructed here were envisioned for use with these larger assemblies (composed purely of DNA), as they were designed to act as the substrates that 'direct' the assembly of these nanowire structures into topologically useful landscapes that will function as smaller computational elements of a larger machine. This is the next logical step towards the development of a truly revolutionary system.

Although not included here, it has been demonstrated that these heterostructured devices are capable of behaving as both sensors and plasmon propagation media. Specifically, Au-CdSe-Au nanowires show a dependence in their conductivity based on the presence of sulfur-containing analytes present in the atmosphere. Partial results of these investigations has been presented at Nano DDS in 2007, and further work would be useful in determining what other analytes these structures may be sensitive to as well. In a collaborative effort, these devices have been used in surface plasmon experiments where it has been demonstrated that plasmons can both propagate from one end of the nanowire and emit at the other. It has also been demonstrated that the intensity of the emitted photons at the end of the nanowire opposite of the incident beam has a dependency on the polarization of the incident light and can be modulated; thus these devices also act as optical switches. The mechanism behind this observed phenomena is not yet clear, and further effort will be required to determine the source of this behavior. Another interesting experiment may be discovering the dependence on mechanical perturbations on the propagation of surface plasmons, which would help provide insight into what level of deformation may be present in any given 'switch' while still allowing a larger computational device to function as expected.

Appendix A

Fabrication of Thin film AAO Templates

A.1 Overview

This section outlines procedures and techniques used to produce AAO templates in house. The information contained here closely mirrors techniques used by other groups found in the literature, although some key differences were adopted that enabled the successful growth of these templates using only a thermal evaporator instead of equipment= (e.g. a sputter coater or an e-beam evaporator) used by others. In particular, a plasma cleaning step was found to be essential to the successful fabrication of thin film AAO templates on glass and silicon substrates. This step has not been stated before in literature and to my knowledge is the first ever recommendation made by anyone that fabricates thin film templates. The mechanism behind this step and why it is crucial for thermally evaporated film is discussed below.

A.2 Introduction

Commercially available AAO templates are ceramic films that are commonly used as filtration devices as this is generally intended as their sole purpose by the manufacturers. These filtration templates are occasionally used by some research groups as templates for nanowire growth when the dimensions of the nanowires are not critical to the experiments performed.(Lee et al., 2006; Skinner et al., 2006; Sehayek et al., 2005) Until recently, Whatman has been the only commercial provider of these templates, which are affordable as each template has a cost of only a few dollars. Researchers that choose to use these templates often obtain the templates with pore sizes of 0.2 μm although templates with pore diameters of 0.1 μ and 0.02 μ are also available from this supplier.

As all researchers that use these templates in their work are aware, these templates nominally have pore diameters that are 0.2 μm, but the actual size of these pores can be a much as 75% larger than what is advertised with diameters approaching 350 nm, with large variations existing in both the batch of templates in a single box and within the template itself. Smaller diameter templates exasperate these variations in diameter even more as the diameters vary from 20 or 100 nm on one side of the template to the 200 to 350 nm diameter variation observed in the nominally 200 nm templates mentioned above. If these variations were only restricted to a small portion of the total available thickness of the template (50 μm, as stated by the manufacturer) these templates could still be usable in research sensitive to both the overall and variation

in the diameters of nanowires produced from these materials. However this isn't the case as is evident in Figure 3.6 since the advertised pore size for the smaller diameter templates are only that size over several hundred nanometers of the total template thickness at best.

Figure A.1: Profile view of a 55 nm pore diameter Synkera AAO template broken in half to expose the pore structure.

Another manufacturer that has recently entered itself into the commercial providers of AAO templates is Synkera. This manufacturer produces AAO templates with an assortment of diameters ranging from 200 nm down to 13 nm, over several template diameters (13 mm and up) and of the same thickness as those provided by Whatman. They can also produce templates on various substrates including glass and silicon, as well as templates with through-hole pores, with the barrier layer intact, or still attached to the original substrate. Effectively, Synkera is in the business of manufacturing AAO templates to meet researchers needs that want to produce nanowires with very tight control over the diameters of the nanowire. Although their templates do effectively

have the advertised dimensions throughout the entire thickness of the template (see Figure A.1, this flexibility does come at a cost however, with prices starting at 40 USD *per template*. Thus, the cost of 4 templates from Synkera will afford you at least 50 from Whatman.

Researchers that do require more precise control over the dimensions of their final nanowires often elect to produce their own templates using custom setups in their labs. Most researchers follow the method pioneered by Masuda(Masuda and FUKUDA, 1995) and use high-purity aluminum foil as their initial substrates for production of their templates,(Sharma et al., 2007; Lombardi et al., 2006; McMillan et al., 2005) although in recent years some researchers have been deviating from this by using other substrates including silicon(Tian et al., 2005) and glass(Evans et al., 2006) with thin films of aluminum deposited on top of these substrates as their starting material. Formation of thin films of aluminum not only allows the researchers to reduce their costs but also allows for fine control over the final thickness of the template after anodization is complete. This permits researchers to reduce the amount of time required for anodization of the template, which proceeds at 150 nm/min for oxalic acid baths under typical anodization conditions.(Wade and Wegrowe, 2005) (Please note that this rate generally depends on anodization voltage, bath composition and temperature.) This fine level of control allows novel experiments to be carried such as surface enhanced raman spectroscopy (SERS) of silver nanowires.(Lee et al., 2006) Although the reproducible and reliable fabrication of nanoparticles with controllable inter-particle spacing is difficult to control via solution based techniques, nanowire based methods have been

shown to circumvent this limitation and is a strong candidate as a sensitive molecular sensing tool coupled with SERS. Other examples of applications resulting from fine control over the length and/or diameters of nanowires range from catalytic nanomotors(Paxton et al., 2004) to nanowires with tunable magnetic properties (Chen et al., 2006) and broadband light emitting diodes.(Bao et al., 2006)

In the fabrication of templates in house at UNC, the method of Masuda was initially followed(Masuda and FUKUDA, 1995), but due to the amount of time required to form our first templates with ordered and regularly sized pores along with the cost of the starting high-purity foils and the amount of time that was required to anodize enough of the foil to produce a substrate that would be mechanically robust enough for handling (typically 18 hours or more), it was eventually decided that alternate methods should be used that would produce the final desired through-hole templates more quickly. The process that was finally settled on produced these templates in as little as 1 hour, and is based on a method devised by Mallouk's group.(Tian et al., 2005)

A.3 Experimental

The procedure used to construct AAO templates with thicknesses as thin as 400 nm followed the method devised by Tian et. al.(Tian et al., 2005) with one exception due to the use of a thermal evaporator in place of an electron-beam evaporator used to deposit titanium and aluminum. Due to the surface roughness of the deposited aluminum films, it was necessary to reduce this mechanism by exposing the substrates

to the plasma of an oxygen plasma cleaner at high power (100 W) for ten minutes. The remainder of the procedure used followed that outlined in the literature.

A.4 Results and Discussion

As this is the first instance of a plasma cleaning step being incorporated into the fabrication of AAO templates, a mechanism is proposed to explain why this additional step permits films that could not otherwise be anodized to be processed successfully after the inclusion of this step. Figure A.2 shows a typical image of thin films ofTi-Al on glass substrates after anodization in 0.3 M oxalic acid for 30 mins that have not been plasma cleaned. This image shows some darker spots on the film that appear to be sites where the formation of pores may have tried to nucleate, but the pores are ill-defined and the spacing is highly irregular. Figure A.3 shows identical substrates that were first exposed to an oxygen plasma for 10-15 minutes before anodization was carried out. Even though Figure A.3 was captured at less than half the magnification of Figure A.2, the pores in the film that was plasma cleaned are clearly visible at only a magnification of 25k. Small regions of Figure A.3 do exhibit some ordering over length scales of a couple hundred nanometers and performing a Fourier transformation on small subregions of this image presents a faint hexagonal pattern which is typical of anodized aluminum films. An example of this is shown in Figure A.5. For comparison, an anodized aluminum film that has undergone a two step process is presented in Figure A.4, where the ordering is present over much larger regions of the film.

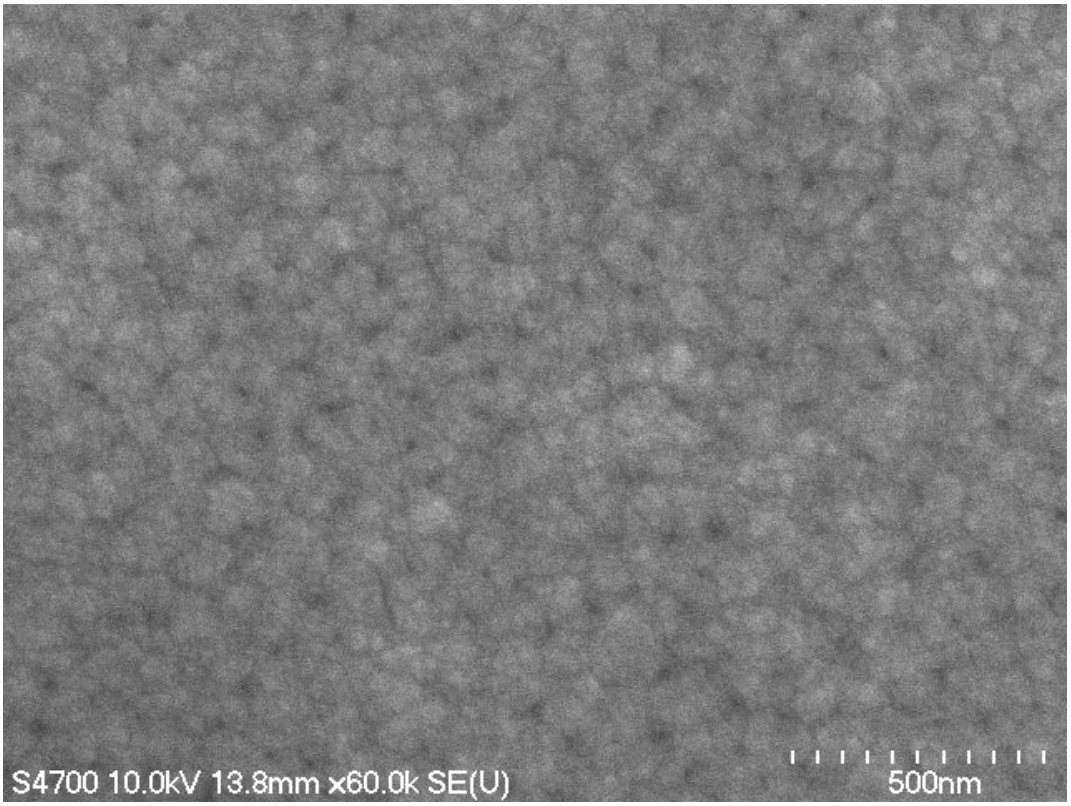

Figure A.2: Thin film thermally evaporated Ti-Al layers after anodization in 0.3 M oxalic acid.

A mechanism for these observable differences between untreated thermally evaporated aluminum films and films that are exposed to an oxygen plasma is now presented. It is proposed that by placing the substrate into a chamber where the only reactive species is oxygen a significant reduction in the surface reduction of the native oxide layer present on the aluminum film is achieved. It is possible that reaction of the surface with an oxygen plasma strengthens weak areas of the oxide present on the substrate sufficiently enough that the subsequent anodization can occur successfully on a film that otherwise would not otherwise yield any pores.

This method of exposing a substrate with a thermally thin film of aluminum to an

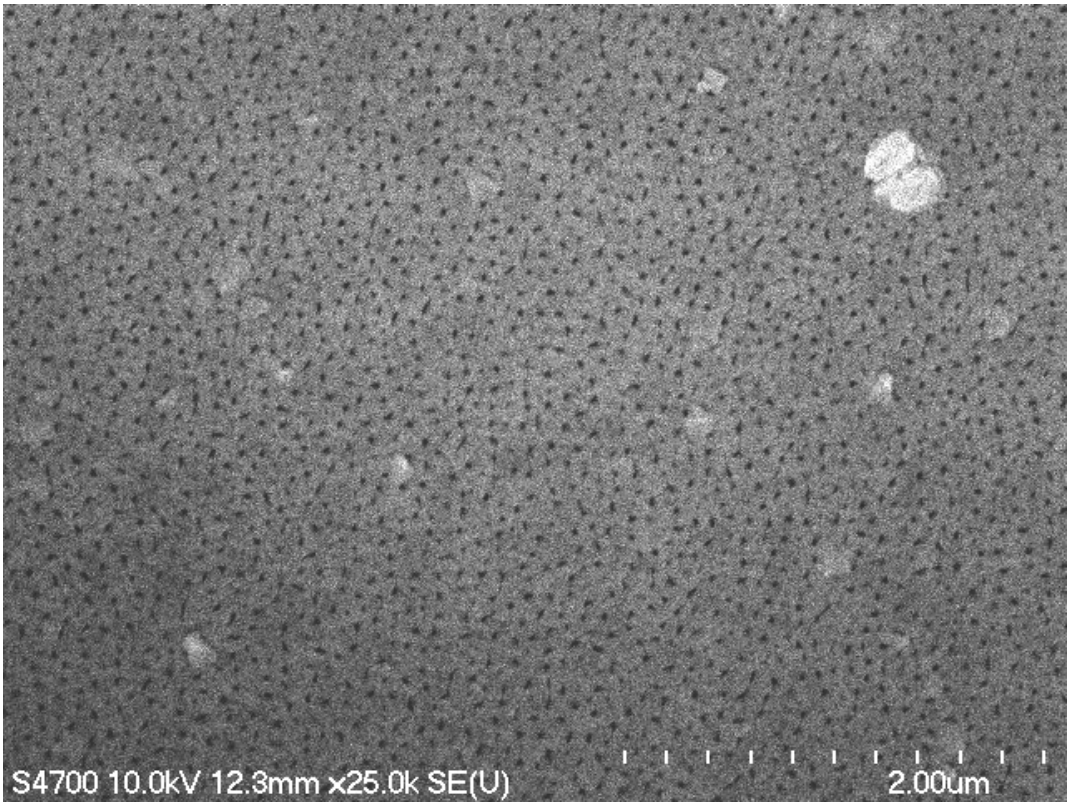

Figure A.3: Thin film thermally evaporated Ti-Al layers with reduced surface roughness by plasma cleaning after anodization in 0.3 M oxalic acid.

oxygen plasma before anodization has allowed films to be anodized producing pores as small as 35 nm (as anodized) and as large as 150 nm. Figure A.6 shows such a thin film after it has been anodized in a 10% phosphoric acid bath that initially contained a 400 nm thick thermally evaporated aluminum layer. In the case where a usual 0.5 mm thick aluminum sheet was anodized that has been exposed to an oxygen plasma before the usual electropolishing step was performed, the aluminum sheet shows the typical hexagonal ordering after anodization that is present only after a two step anodization is performed (Figure A.7). This further reinforces the notion that exposure of the aluminum film to an oxygen plasma reduces the surface roughness similar to surfaces

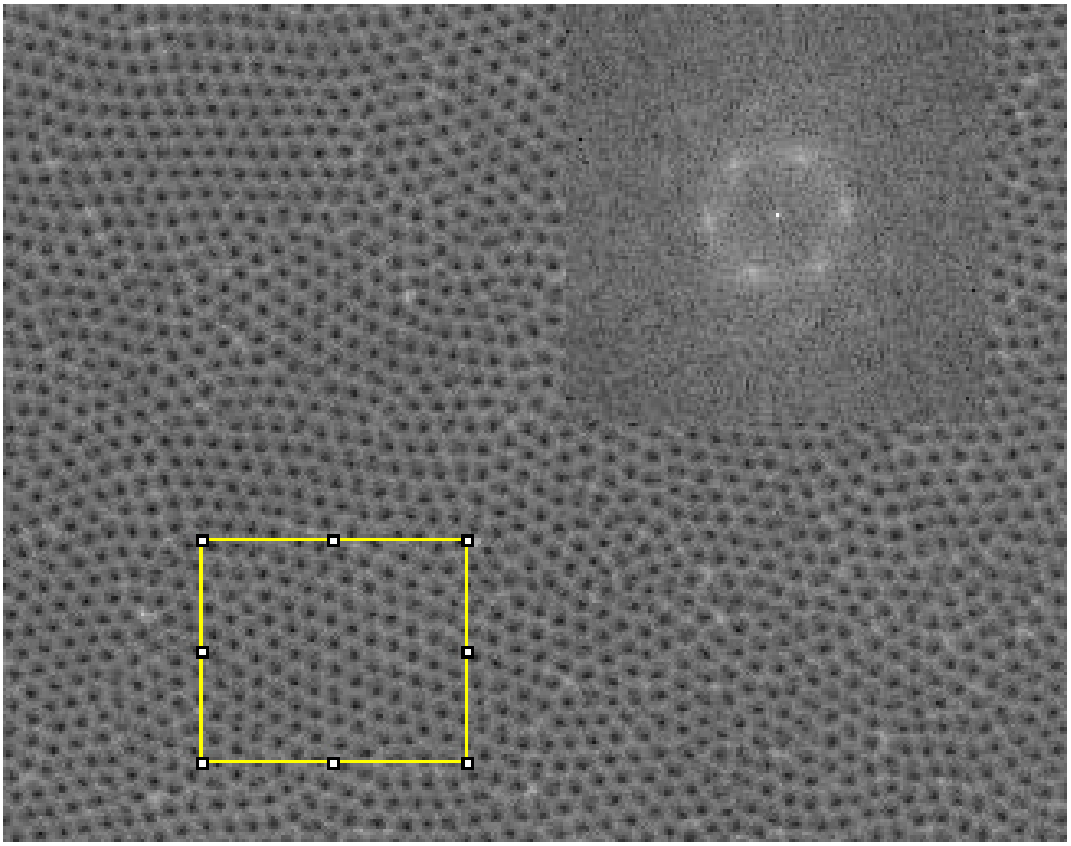

Figure A.4: SEM micrograph at 13k of an aluminum oxide thin film anodized in 0.3M oxalic after two step anodization. The pores are ˜50 nm. The inset is a 128 x 128 pixel sub-region of the boxed yellow area in the main image. Note the regions of hexagonally arranged pores over large domains, as is indicated by the pattern visible in the FFT.

of aluminum films that have already undergone one step of anodization and have then had their alumina surfaces removed before the second anodization step. Films at this step display low surface roughness compared to their non-anodized counterparts.

In conclusion, this section outlines the successful integration of a technique that permits thin films of aluminum to be anodized for the successful fabrication of porous aluminum oxide with pores perpendicular to the anodization surface. Inclusion of an oxygen plasma step not only decreases the processing time required for the production

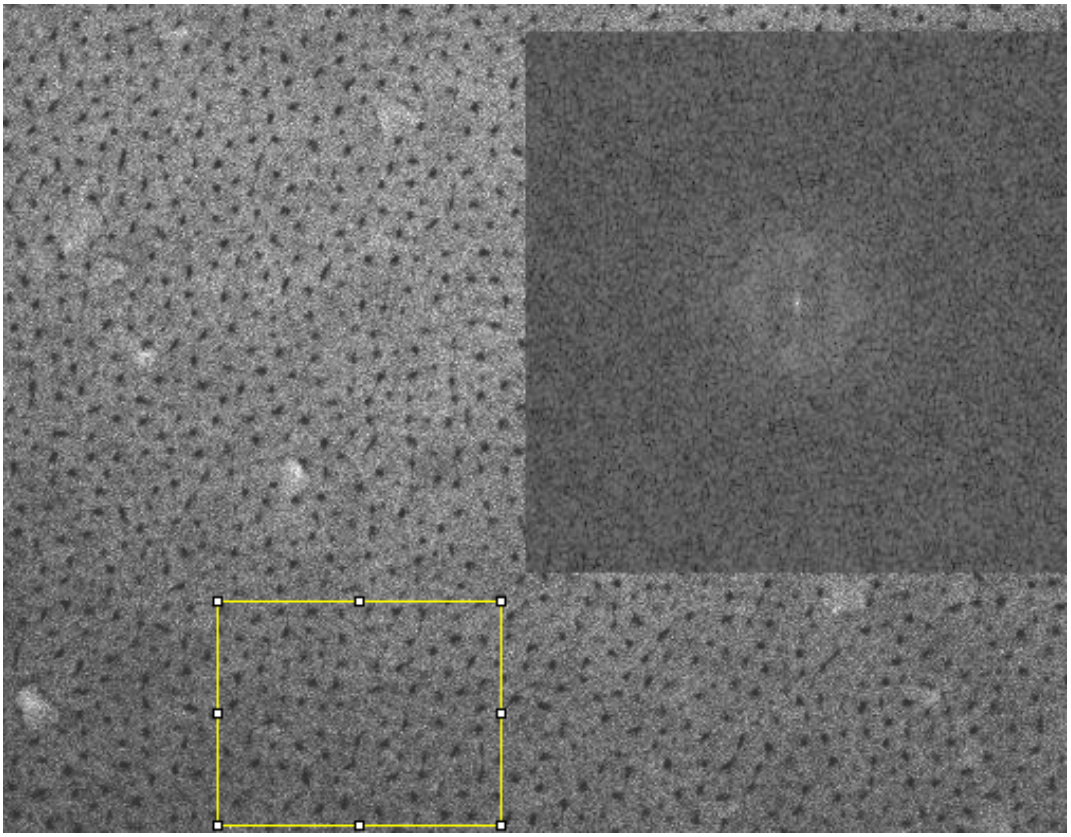

Figure A.5: SEM micrograph at 25k of an aluminum oxide thin film anodized on glass in 0.3M oxalic after oxygen plasma treatment. The inset is a 128 x 128 pixel sub-region of the boxed yellow area in the main image. Although a hexagonal pattern can be discerned from the inset, the ordering is significanly less pronounced here than in the inset of Figure A.4.

of these films but also increases the ordering of the pores formed in these films. This may find use in areas where ordered (or semi-ordered) nanowires embedded in optically transparent substrates are required.

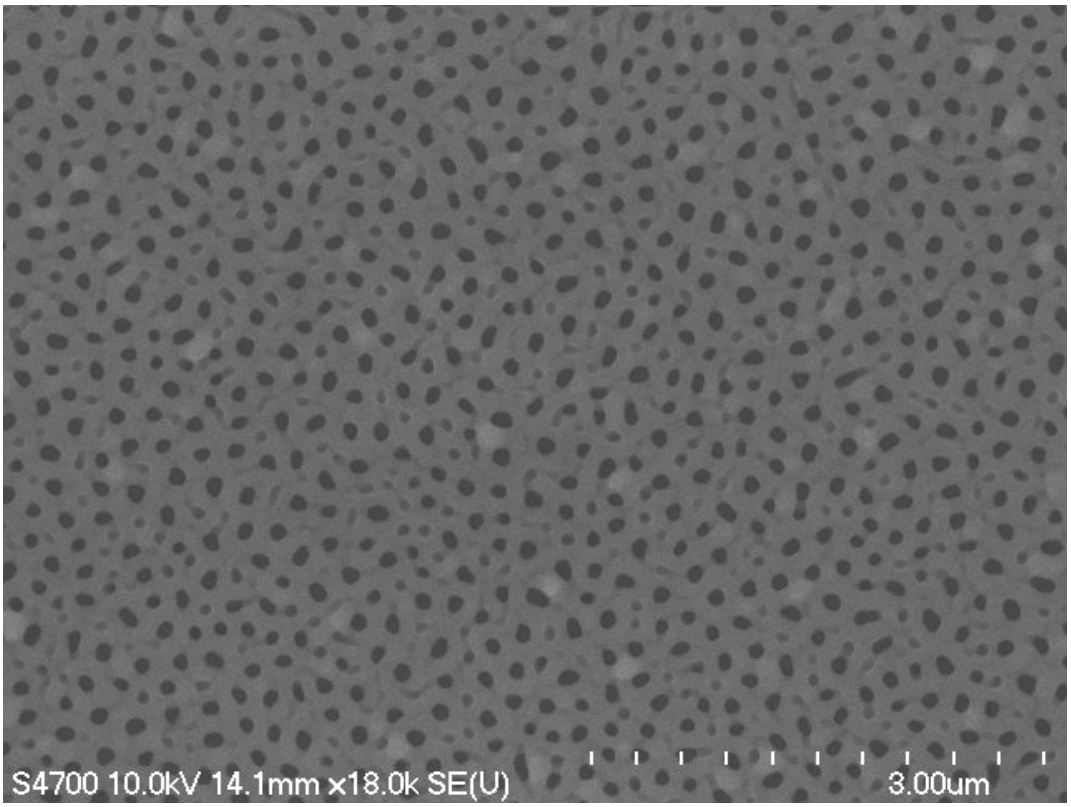

Figure A.6: SEM micrograph at 18k of an aluminum oxide thin film anodized on glass in 10% phosphoric after oxygen plasma treatment. The pore sizes are ˜150 nm.

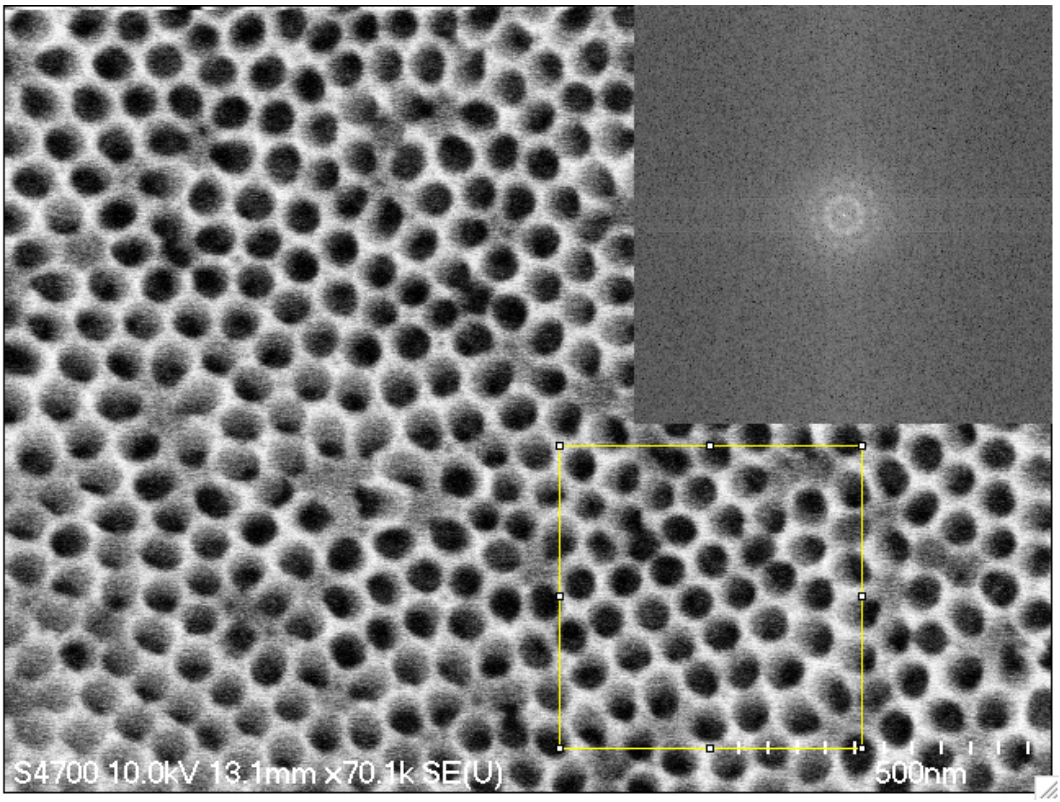

Figure A.7: SEM micrograph at 70k of an aluminum sheet (0.5 mm thick) exposed to an oxygen plasma after the first anodization step in 0.3 M oxalic acid.

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